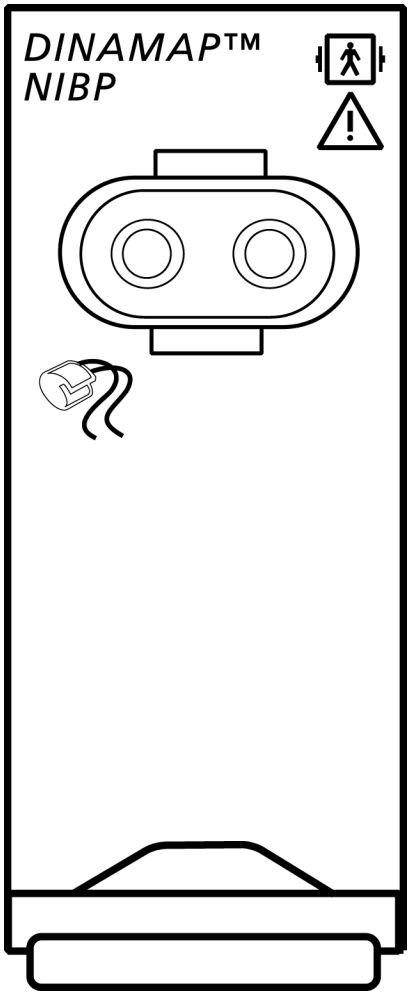
NIBP SINGLEWIDE MODULE

INTRODUCTION

This area contains component information about the singlewide Model 7300 Non-Invasive Blood Pressure (NIBP) Module. The singlewide NIBP module monitors blood pressure noninvasively, using the oscillometric method that measures the amplitude of the pressure oscillations within the blood pressure cuff. Systolic pressure, diastolic pressure, mean arterial pressure, and cuff pressure are all measured by the module. Heart rate values are also derived from the pulse rate determined by the oscillometric blood pressure measurement technique.



PHYSICAL DESCRIPTION

The singlewide version of the NIBP module, shown in FO-42B, occupies a single module slot. The module consists of two PWAs, interconnect cabling, a pump manifold assembly, a cuff manifold assembly, and a mechanical enclosure. Digital PWA 315459 includes an interface to the PNet communication bus, module core logic, and the analog to digital conversion subsystem.

Analog PWA 315452 includes the pressure transducer amplifiers and filter circuitry, pneumatic system overpressure detection circuit, and the pneumatic valves and pump control. The digital PWA, with its PNet connector, occupies the left slot in the module enclosure when viewed from the sensor connector end (front) of the module. The analog PWA occupies the right slot in the module enclosure.

Flex cable W100 connects the digital and analog PWAs. It is soldered to the analog PWA, and attaches to a pin header on the digital PWA. Flex PWA 313-113 connects the analog PWA to transducer XD2, mounted on the cuff manifold assembly. Flex PWA 313-114 connects the analog PWA to transducer XD1, mounted on the pump manifold assembly. Cable assembly W102 connects the analog PWA to the pump, zero/deflate valve, and dump valve mounted on the pump manifold assembly.

FUNCTIONAL PRINCIPLES OF OPERATION

A schematic diagram of the pneumatics system is shown in Figure 4-1. It illustrates all connections to valves, transducers, and pump. The pump draws air in and forces it through the check valve to the system manifold. The filtered orifice is used to bleed off air in the chamber between the pump and check valve. This allows the pump to start up without back pressure. The check valve prevents pressurized air in the system from going back through the pump when it shuts off. Transducer XD2 monitors the total system pressure and provides an overpressure signal to the analog PWA when the pressure gets too high. During an overpressure condition, deflate/zero valve V2 energizes and vents the pressurized air to the atmosphere. Transducer XD1 monitors pressure through the cuff during a blood pressure measurement. After the blood pressure measurement is complete (or after power failure), dump valve V3 deenergizes and vents the pressurized cuff to the atmosphere.

A functional block diagram of the NIBP Singlewide Module is shown in FO-42A. The diagram is divided into analog circuits and core logic circuits. The analog circuits are shown in the top half of sheets 1 and 2 and the core logic circuits are shown in the bottom half of sheets 1 and 2.

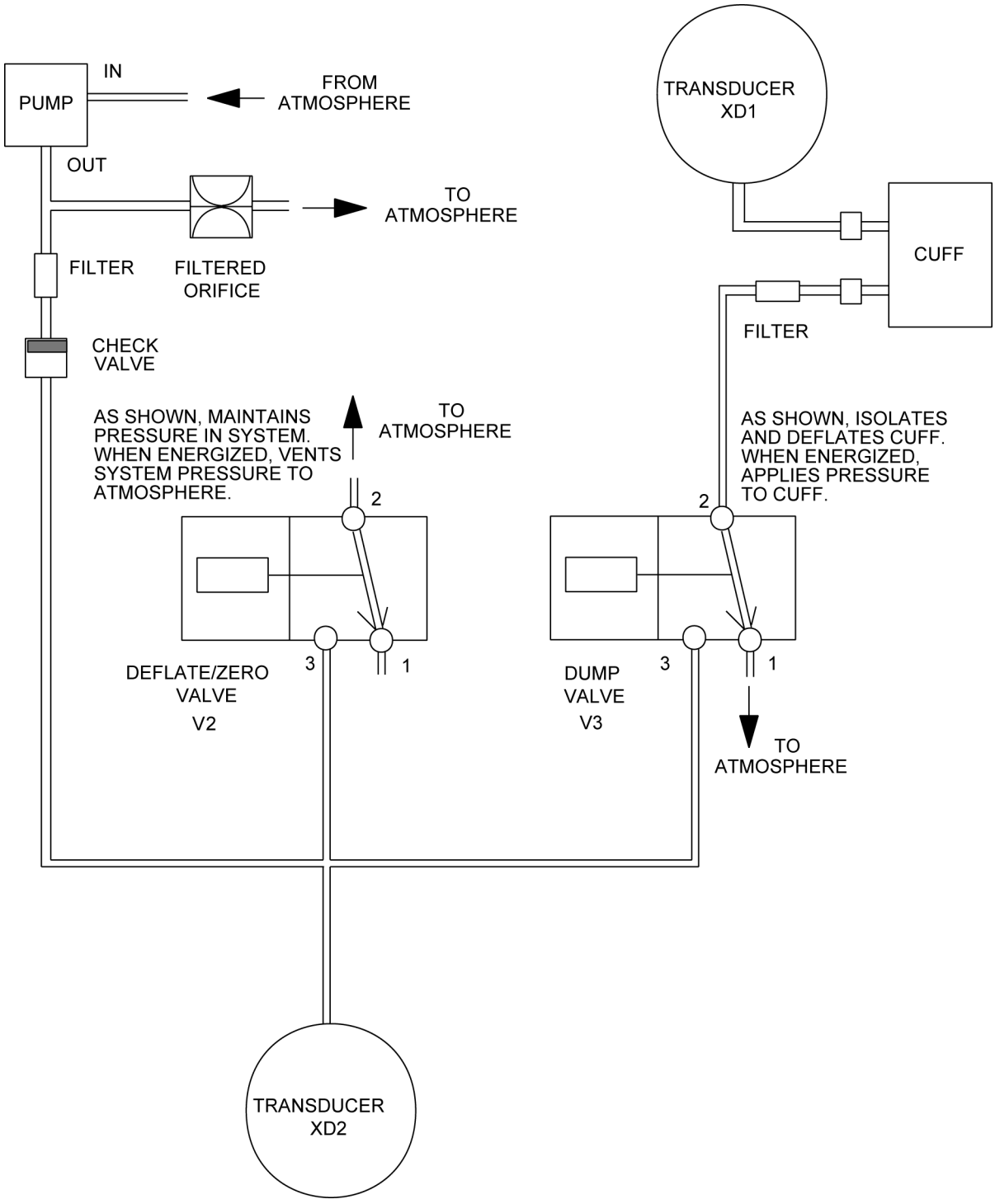


Figure 4-1. NIBP Singlewide Pneumatics Schematic

Analog Circuits

The analog circuits consist of cuff measurement, overpressure, and pneumatics circuits. Transducers XD1 and XD2 shown on sheet 1 receive excitation voltage from +10V references. Differential signal XD1SIG+/- from transducer XD1 representing blood pressure is applied to the analog multiplexer through the pre-amp and low pass filter. The pre-amp is gain controlled and the filter removes any erratic and false data from the signal.

Differential signal XD2SIG+/- representing system pressure from transducer XD2 is applied to the overpressure amplifier. Overpressure threshold is programmed by the CPU to a specific level. This threshold level and the actual system pressure are summed together by the summing amplifier and applied to the delay circuit. This built-in delay prevents a false overpressure caused by transient surges in the system pressure. The overpressure threshold control also allows selection of either neonatal or adult pressure limits via ADULT-0 signal. This signal is true when an adult cuff is attached, and false when a neonatal cuff is attached.

The CPU addresses the analog multiplexer through ASEL0 through ASEL2. This allows the multiplexer to poll any of seven inputs (AIN1 through AIN7). Thus, the multiplexer monitors transducer references and outputs, system pressure and overpressure, and pump drive outputs. This multiplexed analog signal (BUF_ANA_MUX) is converted to digital by the A/D converter and sent to the CPU for evaluation and response.

The pneumatics decode logic circuits shown on sheet 2 provide a logical sequence of inflation after receiving a RESET-0 signal. CLAMP1 and CLAMP2 signals control the transducer gain circuits shown on sheet 1. ADULT-0 signal is generated when an adult cuff is attached, and provides higher overpressure limits. This logic also controls the pneumatics latch and solenoid drive circuits.

The pneumatics latch and solenoid drive circuits control the pump drive and the dump and deflate/zero valves. Pneumatic reset or failsafe signals from the CPU shut down the pump and open the dump valve. Signal PUMPC measures pump current. This allows the CPU to monitor when the pump is running. DEFLATE_VAL signal from the pneumatics latch and solenoid drive circuit energizes deflate valve V2, releasing cuff pressure. DUMP_VAL signal deenergizes dump valve V3, releasing all system pressure. Both valves receive +12V power from the analog PWA.

Core Logic Circuits

The core logic circuits are shown on sheet 2 of FO-42A. Functional blocks include the PNet interface, reset/failsafe, 68302 CPU, 128Kx8 data memory, 128Kx8 program memory, the model and serial number EEPROM, and logic analyzer/test interface.

The Module will not be damaged when plugged into a live slot. Core logic power inputs to a Module are limited to a peak inrush current during hot-plugging. Within 2 seconds the Module will respond to identification and wake up in a minimized power state until registered with the system.

The PNet interface allows asynchronous and synchronous data transfer between the core logic and the external devices. Synchronous operation is always used in MPS systems. Asynchronous operation is for test and development only. The reset/failsafe logic provides power-on reset, processor reset and halt, and failsafe if a problem occurs with the microprocessor. The microprocessor controls and transfers data within the core logic. The program memory is a FLASH device that can be loaded with program information from the PNET interface or the logic analyzer interface. Data memory temporarily stores status and monitoring data for processing.

COMPONENT PRINCIPLES OF OPERATION

The following paragraphs describe the function of the two rigid PWAs. The NIBP analog PWA provides the circuitry for the excitation, amplification, and signal conditioning (filtering) for measurement of non-invasive blood pressure within the NIBP module. Also included are the associated circuitry for a separate, independent direct overpressure interactive channel. The NIBP digital PWA provides the processor, communication, and analog to digital conversion for the NIBP module. Schematic diagrams SC315-452 and SC315-459 are provided.

The mapping of signals located in the CPU Port Register A and Port Register B are listed in Table 42-1.

Table 42-1. CPU Register Mapping

Mapping of Bits in Port A:

Bit	Signal	Type	Comment
PA(0)	SCC2 RXD	input	debug serial data to
PA(1)	SCC2 TXD	output	debug: serial data from
PA(2)	SP_CS	output	Enable for Serial EEPROM
PA(3)	Failsafe-1	input	Monitor status of Failsafe latch
PA(4)	PNEURESET	output	Pulsed low-high-low to reset
PA(5)	ASYNC-EN	output	Selects Com Mode for PNET, H=Async
PA(6)	MOTOR_PWR_CNTL	output	Delayed Power to Motor & Valves
PA(7)	LATCHED_OVC	input	Latched Over_Current, normal=1
PA(8)	DATA FROM ISO	input	(Unused)
PA(9)	DATA TO ISO	output	(Unused)
PA(10)	SPARE 1		
PA(11)	ADCLK	output	SCC3 (TxCLK)
PA(12)	UFIL_OVP-0	input	Unfiltered Overpressure (OVP-0)
PA(13)	ASEL0	output	Analog Mux -LSB
PA(14)	ASEL1	output	Analog Mux
PA(15)	ASEL2	output	Analog Mux -MSB

Table 42-1. CPU Register Mapping (Continued)

Mapping of Bits in Port B:

Bit	Signal	Type	Comment
PB(0)	LATCH_OVP	input	Latched Overpressure, normal =1
PB(1)	POTCS-0	output	init_val =1
PB(2)	POTINC-0	output	init_val = 1
PB(3)	POTU~D-0	output	init_val = 0
PB(4)	TOUT1-0	output	(Not used)
PB(5)	TIN2	input	**Debug Only
PB(6)	PT1_CLAMP-0	output	init_val = 1
PB(7)	WDOG-0	output	WatchDog Timer, normal =1
PB(8)	FPTTST-0	output	init_val = 1
PB(9)	ADCBUSY-0	input	busy = 0
PB(10)	SYNC-0	input	PNet
PB(11)	SELECT-0	input	PNet

Analog PWA

The NIBP analog PWA includes four functional circuits: analog mux, filtered NIBP, overpressure, and pneumatics.

Analog Mux

The analog mux functional block consists of a single eight-to-one analog multliplexer and includes an output buffer amplifer. Data is transferred to the digital card via a single analog channel BUF_ANA_MUX (MUX_OUT) on J100, Pin2. Channel selection is defined by three address lines ASEL0-ASEL2 in connector J100. These channel assignments are defined in Table 42-2.

Table 42-2. Analog Multiplexer Channel Assignments

Channel	ASEL0	ASEL1	ASEL2	Signal	Description
AIN0	0	0	0	MOTRC_REF	Motor Current Limit Ref Voltage
AIN1	1	0	0	TH_VREF	Overpressure Threshold Voltage
AIN2	0	1	0	PT2	Unfiltered Manifold Pressure
AIN3	1	1	0	PT2_REF	XDCR2 Excitation Voltage Ref
AIN4	0	0	1	FPT1	Filter Cuff Pressure
AIN5	1	0	1	PT1	Unfiltered Cuff Pressure
AIN6	0	1	1	PT1_REF	XDCR1 Excitation Voltage Ref
AIN7	1	1	1	PUMPC	Pump Current Sense Voltage

Filtered NIBP

The filtered NIBP functional block consists of signal conditional circuitry required to measure the cuff oscillatory pressure (PT1) and acquire a blood pressure determination. Circuitry for offset, voltage clamping, and test pulse injection are also included. The excitation voltage for the cuff transducer is derived from the analog-to-digital converter, located on the digital PWA. Changes in the A/D derived reference produce a ratiometric change in the channel and tend to compensate for the initial reference change.

A +350mV nominal offset is added to the PT1 channel to insure its signal remains positive, since the A/D converter input signal is limited to a uni-polar, 0 to 5.0 Volts range. The FPT1 channel has a +200mV nominal offset.

The pulse component (typically one percent) of the cuff pressure signal is separated from the cuff pressure signal by a cascaded high-pass filter section followed by a low-pass filter section. Each filter section contains two poles. The passband of this filter is nominally 0.5 to 7.2 Hz. Testing of filter characteristics is accomplished using the FSTTST signal.

The blood pressure algorithm requires the ability to initialize (clamp) the high pass filter in the process of separating and measuring the pulse signal. Two clamps are used in this process. FLT_Clamp-0 provides a clamp to ground of the input to the second stage and also clamps the output buffer to a +200 mV offset reference voltage. The second clamp, PT1_Clamp-0 is used to isolate the input channel to zero. This clamp is applied to disconnect the input pressure transducer signal from the channel. This permits a true, uncorrupted test signal to be injected in to the input of the channel to measure filter characteristics. This test pulse is accomplished by toggling the FPTTST-0 signal. FPTTST-0 should normally be held HIGH, otherwise it will inject a nominal offset of 37.5 mV in the PT1 channel.

The inputs to both pressure measurement channels PT1 and PT2 are derived from a pressure transducer having the characteristics defined in Table 42-3. Table 42-4 defines the range of parameter variations for the cuff measurement channel.

Table 42-3. Transducer Characteristics

Operating Conditions: Excitation voltage = +10.000V

Characteristics	Symbol	Min	Typ	Max	Units
Pressure Range	P	0		375	mmHg
XDCR,FSS	VFSS	38.5	40	41.5	mV
XDCR, OFFSET	VFSS	-1.0		+1.0	mV
Linearity, of XDCR		-0.25		+0.25	%FSS

FSS == Full Scale Span

Table 42-4. PT1 Output Characteristics

Operating Conditions: Power Supply Voltages=+5V+/-5%, +12V+/-5%, -12V+/-5%

Characteristics	Symbol	Min	Typ	Max	Units
Gain*	G2	88.83	91.89	94.96	
Offset	Voff	335	349	363	mV
Offset, including AD2 ref	Voff	326	349	372	mV
XDCR,FSS	VFSS	38.5	40	41.5	mV
XDCR, OFFSET	VFSS	-1.0		+1.0	mV
Linearity, with XDCR		-0.25		+0.25	%FSS
Full Scale Scan, with XDCR	VFSS	3511	3676	3842	mV
Offset Voltage, with XDCR	Voff	178	349	495	mV

*Gain of signal [range 1-40mv] injected between pins J103-Pin4 and J103-Pin2

Overpressure

The overpressure circuit generates a separate, independent pressure measurement channel (PT2), including its own separate excitation voltage source (Table 42-5). Also included is circuitry for electronically setting the overpressure threshold point. Both the excitation reference voltage PT2_REF and the unfiltered pressure transducer (PT2), which is amplified and buffered, are available as output to the A/D converter. The PT2 channel also has a +350 mV offset voltage injected to insure the uni-polar A/D converter input always remains positive (Table 42-6).

Table 42-5. PT2 Output Characteristics

Operating Conditions: Power Supply Voltages = +5V+/-5%, +12V+/-5%, -12V+/-5%

Characteristics	Symbol	Min	Typ	Max	Units
Gain*	G2	90.70	91.89	93.08	
Offset	Voff	339	349	359	mV
Linearity, with XDCR		-0.25		+0.25	%FSS
Full Scale Scan, with XDCR	VFSS	3555	3676	3904	mV
Offset Voltage, with XDCR	Voff	178	349	495	mV

*Gain of signal [range 1-40mv] injected between pins J103-Pin3 and J103-Pin5

Table 42-6. Reference Output Characteristics

Operating Conditions: Power Supply Voltages = +5V+/-5%, +12V+/-5%, -12V+/-5%

Characteristics	Symbol	Min	Typ	Max	Units
PT1 Reference Voltage	PT2_REF	3253	3329	3406	mV
PT2 Reference Voltage	PT2_REF	3253	3329	3406	mV
FPT1 Reference Voltage	FPT1	170	200	230	mV
OverPressure Threshold Voltage	TH_VREF				
Adult Mode		2952	3290	3700	mV
Neonate Mode		1364	1530	2047	mV
Motor Over Current Ref Voltage	MOTR_C_Ref	2424	2500	2574	mV
PT1 EXCITATION Voltage	EXC1+		10.000		V
PT2 EXCITATION Voltage	EXC2+		10.000		V

The excititation reference voltage for transducer PT2 is used to generate a threshold voltage to compare with the actual pressure of the cuff as measured by transducer PT2. The reference voltage is buffered by an adjustable gain amplifier to produce the reference pressure point of 300 mmHg (150 mmHg in neonate mode) for the trip point. The amplifier gain is altered by modifing the feedback resistance of the amplifier by means of a solid state non-volatile, digital E2POT. The digital E2POT has a resolution of 100 steps. Total adjustment trim range is limited to about +/-10%.

Threshold trimming is accomplished by controlling three input signals: CS-0 (Chip Select), U_D-0 (Direction: Up or Down), and INC-0 (Increment or Decrement). A interlock jumper, JP1, which connects CS-0 to the board edge pin, is required to be installed or threshold adjustment is inhibited. The E2POT incorporates a storage mode that permits maintaining the threshold setting once adjusted. The last state saved is recalled from non-volatile storage on system power-on, returning the overpressure threshold point to the previous set point.

Pneumatics

The pneumatic functional block includes the control signal decode logic, the valve driver circuitry, the pump driver circuitry, pump current measurement circuit, and a safety interlock circuit.

Control signals for the board are derived via three different sources: direct control from registered outputs of the processor, controls signal derived from processor address write commands (which are stored in an addressable latch), signals derived from the watchdog timer, and signals generated by the overpressure functional block. The four valve control signals and the pump control signal are derived from the write address and stored in an addressable latch. The latch signals are defined in Table 42-7. Latch values are cleared by application of system RESET generated by the processor. Refer to Table 42-8 for reset conditions. Each latch signal is individually gated in a programmable logic device (22v10) with the fail safe input signal (watchdog timer) and the overpressure latch output to ensure pressure is removed from the patient cuff should either overpressure or processor hang-up condition occur.

Table 42-7. Latched Control Signals and Decode Matrix

Operating Conditions: RESET-0 =1; PNEURESET=1; FAILSAFE-0 =1; FLT_0VP-0=1

Pneu_Enab	Data	LSEL0	LSEL1	LSEL2	Signal	Value	Description
¥	0 1	0	0	0	TK_Inflate_Val	Open Closed	Not Used
¥	0 1	0	0	0	Cuff_Deflate_Val	Closed Open	When open, deflates Cuff
¥	0 1	1	0	0	Cuff_Dump_Val	Open Closed	When closed, dumps pressure in Cuff
¥	0 1	1	0	0	Pump	OFF ON	When ON, activates PUMP
¥	0 1	0	1	0	Unload_WD	ON OFF	Pneumatic Watchdog Signal
¥	0 1	0	1	0	OVP_MODE ‡	OFF ON	Controls Overpressure Mode
¥	0 1	1	1	0	FLT_Clamp-0 ‡	OFF ON	When ON , Injects Offset into Filtered Channel Output
¥	0 1	1	1	1	Adult ‡	Adult Neonatal	When ON, Selects Neonatal for OP Threshold Voltage Ref

¥ == negative pulse condition
‡ == independent of pneureset, failsafe, flt_ovp

Table 42-8. System Reset State

Operating Conditions: PNEURESET=1; FAILSAFE-0 =1; FLT_0VP-0=1

Reset	Data	LSEL0	LSEL1	LSEL2	Signal	Value	Description (Reset Condition)
0	X	X	X	X	TK_Inflate_Val	Open	Not Used
0	X	X	X	X	Cuff_Deflate_Val	Closed	Valve UnEnergized
0	X	X	X	X	Cuff _Dump_Val	Open	Valve Energized
0	X	X	X	X	Pump	OFF	PUMP
0	X	X	X	X	FLT_Clamp-0	ON	Clamped
0	X	X	X	X	Adult	Adult	Over Pressure = Adult Level
1	X	X	X	X	Latched_OVP	HIGH	Cleared Low if HIGH Fil-OVP Occurred
1	X	X	X	X	Latched_OVC	HIGH	Cleared Low if Motr-OVC

A cross coupled latch for overpressure is included in the programmable logic device. It is set by the occurrence of an overpressure condition existing for a period greater than 500 milliseconds, nominally. When this condition occurs, Filter_OVP-0 transitions low setting the internal latch. The latch output state is indicated by the Latched_OVP signal. The latch can only be cleared by an occurrence of a PNEURESET pulse. Refer to Tables 42-9 and 42-10 for additional clarification.

Table 42-9. Processor Pneureset State

Operating Conditions: RESET=1; FAILSAFE-0 =1; FLT_0VP-0=1

PneuReset	Data	LSEL0	LSEL1	LSEL2	Signal	Value	Description (Reset Condition)
§	X	X	X	X	TK_Inflate_Val	Vn+1 = Vn	Not Used
§	X	X	X	X	Cuff_Deflate_Val	Vn+1 = Vn	Same, before and after pulse
§	X	X	X	X	Cuff_Dump_Val	Pn+1 = Pn	Same, before and after pulse
§	X	X	X	X	Pump	Vn+1 = Vn	Same, before and after pulse
§	X	X	X	X	Latched_OVP	HIGH	Set
§	X	X	X	X	Latched_OVC	HIGH	Set

§ == positive pulse condition

Table 42-10. Overpressure and FailSafe States

Operating Conditions: RESET=1

PneuReset	Filtered_OVP	FailSafe	Signal	Value	Description
X	0	X	TK_Inflate_Val	Open	Not Used
X	0	X	Cuff_Deflate_Val	Closed	Valve Energized
X	0	X	Cuff_Dump_Val	Open	Valve UnEnergized
X	0	X	Pump	OFF	PUMP
X	0	X	Latched_OVP	LOW	LOW is active
X	0	X	Latched_OVC	HIGH	LOW is active
X	1	0	Tk_Inflate_Val	Open	Not Used
X	1	0	Cuff_Deflate_Val	Closed	Valve Energized
X	1	0	Cuff_Dump_Val	Open	Valve UnEnergized
X	1	0	Pump	OFF	PUMP UnEnergized
X	1	0	Latched_OVP	Ln+1 =Ln+1	Unchanged
§	1	1	Tk_Inflate_Val	Vn+1 = Vn	Not Used
§	1	1	Cuff_Deflate_Val	Vn+1 = Vn	Same, before and after pulse
§	1	1	Cuff_Dump_Val	Vn+1 = Vn	Same, before and after pulse
§	1	1	Pump	Pn+1 = Pn	Same, before and after pulse
§	1	1	Latched_OVP	HIGH	High is inactive
§	1	1	Latched_OVC	HIGH	High is inactive

§ == positive pulse condition

Digital PWA

The NIBP digital PWA block diagram is shown in sheet one of hierarchical schematic SC315-459. It includes the core logic blocks PNET IF (PNET Interface), RESET-FS (Reset - FailSafe), UP8-144 (microprocessor-8 bit), EIGHT BIT MEMORY, and LOGIC ANALYZER TEST IF.

Unique to this PWA is the analog-to-digital converter functional block. The NIBP digital PWA is based on the eight bit version of the module core logic. The microprocessor clock frequency is 19.5104 MHz.

Analog to Digital Converter Functional Block

The analog to digital converter functional block includes the analog to digital converter, bus isolation logic, and a buffer to condition the precision voltage reference. The analog to digital converter is a twelve bit successive approximation, with an internal track/hold and reference. Input range is zero to +5.000 V, establishing a LSB value of 1.22 millivolts. The internal reference is, -5.000 V, is filtered and inverted to provide a +5.000V reference, labeled VREF. The ADC is powered by the +5V rail and the -12V rail. An eight wide data bus (DATA0 - DATA7) connects the ADC to the microprocessor. Data transfers consist of two consecutive byte transfer per data point conversion. The data bus is isolated with a three state buffer to reduce bus noise in the converter. With a 1.219 MHz clock on ADCCLK, conversion time is 10.667 microseconds.

Processor Digital I/O and Chip Select Assignments

68302 PORT	SIGNAL	I/O TYPE	COMMENT
PA0	debug serial SCC2 RXD	output	
PA1	debug serial SCC2 TXD	input	
PA2	SERIAL EEPROM CS	output	
PA3	undefined		
PA4	PNEUMATIC RESET	output	
PA5	ASYNC_EN		(PNET)
PA6	Motor Power Control	output	
PA7	LATCHED_OVC	input	Latched Motor Overcurrent Indication
PA8	DATA FROM ISO		(FOR FUTURE TEMP I/F)
PA9	DATA TO ISO		(FOR FUTURE TEMP I/F)
PA10	SPARE 1		
PA11	ADCLK	output	AD Converter clock
PA12	UNFIL_OVP-0	input	Latched Overpressure Indication
PA13	analog mux sel 0	output	
PA14	analog mux sel 1	output	
PA15	analog mux sel 2	output	
PB0	LATCH OVERPRESSURE	input	
PB1	POTCS-0	output	
PB2	POTINC-0	output	
PB3	POTU~D-0	output	
PB4	undefined		
PB5	timer 2	input	(FROM LA I/F)
PB6	CLAMP3-0	output	
PB7	WATCHDOG TIMER	output	
PB8	FPTTST-0	output	
PB9	ADC BUSY-0	output	
PB10	undefined		
PB11	SELECT-0	input	(PNet)
CS0	FLASH ROM		
CS1	Static RAM		
CS2	ADC_CS		
CS3	PNEU_ENAB-0		

Core Logic

The core logic is shown on sheets 2 through 7 of the schematic. The core logic provides communication between the system host and Module through the PNet synchronous serial interface. The Module is an 8-bit version of the core logic, with one 128Kx8 RAM and 128Kx8 ROM device. The microprocessor runs at 19.5104 MHz.

PNet Interface. The PNet interface, shown on sheet 2 of the schematic, provides the following functions:

- RS485 drivers (U7 and U8) for serial data and clock,
- Module select and presence detection (U2),
- Module synchronization.

Core signals are received on PNet connector J1 (sheet 2) with the following pin-out:

PIN	NAME	PIN	NAME
1A,1B	+5V	6B	M_SELECT
2A	DATA+	7A	M_PRESENT
2B	DATA-	7B	TXOC-0
3A,3B	+3.3V	8A	M_SYNC-0
4A	CLK+	8B	-12V
4B	CLK-	10A,10B	+12V
5A,5B	GROUND	1,2	GROUND
6A	M_RESET		

The NIBP Module is designed to be hot-plugged, or inserted and removed from powered systems. Ground pins 1 and 2 are longer than the other connector pins, thus they make first and break last to protect circuitry. This is partially because of protective impedance located on the system backplane, in series with the Modules +5V and +12V power. Also series impedance on PNet control lines limits inrush and protects logic devices from excessive currents during a hot-plug power up.

The PNet protocol defines two modes of operation: synchronous and asynchronous. The normal mode of operation is synchronous, with half duplex transmitted and received data on differential signals DATA+ and DATA-. As shown on sheet 2 of the schematic, the device transmitting the serial data also generates differential clock signals CLK+ and CLK-. Transceiver direction for data and clock are controlled by the 68302 processor-generated TX_EN-0 (low true transmit enable) signal through U2. In the synchronous mode, both data and clock transceivers U7 and U8 are set to receive (i.e., transmit disabled) when fail-safe signal FS-0 is asserted.

The alternate serial mode, full duplex asynchronous, is entered by asserting processor generated control bit ASYCH_EN. This mode transmits data onto the differential signals CLK+ and CLK-, and receives data from the differential signals DATA+ and DATA-. The transmitter in the Module is disabled unless the Module has been commanded to transmit per the PNet protocol. The Module transmitter is immediately disabled after the last character of a transmission has been sent.

The Module select input (M_SELECT, hi true) instructs the Module to respond to identification requests. When both M_SELECT input and M_RESET input (hi true) are asserted, a Module performs a hardware reset.

The Module present output, M_PRESENT is connected to M_SELECT through diode CR1 to allow a means of determining if the Module is plugged into an instrument. When M_SELECT is asserted (pulled hi) M_PRESENT is hi true.

Module transmitter open collector signal TXOC-0 from Q1 signifies the Module transmitter is enabled. Serial data is then transmitted in the synchronous mode.

M_SYNC is used for timing of shorter latency periods than supported by the serial data protocols. A Module only asserts M_SYNC when enabled by the host.

Reset Logic. The reset logic is shown on sheet 3 of the schematic. Reset logic U9 generates a power-on-reset when power is applied. RESET-0 AND HALT-0 signals remain low for minimum of 130 msec after all logic voltages are in specification.

External reset, processor reset, and halt signals are low for minimum of 24 clocks when external reset asserted. Power monitoring, processor reset, and halt signals low if logic voltages drop below specification. They remain low for minimum of 130 msec after logic voltages return to the specified range.

The reset circuit (U6-4,5,6; U6-11,12,13) provides open drain outputs to the processor bi-directional reset and halt signals.

Fail-safe Logic. Fail-safe latch (U6-1,2,3; U6-8,9,10) ensures that the Module enters a safe state if the processor fails to operate correctly. The latch is set by a low true output from the processor watchdog timer (WDOG-0). The data transmitter is disabled, isolated power is shut down, and the Module remains in a safe state until the latch is cleared by a power on or external reset.

Microprocessor. The core logic design is based around the 68302 microprocessor (U10) shown on sheet 4 of the schematic. The 68302 combines a 68000 core with a three channel communication processor, and system integration circuits.

The left side of the CPU contains clock interfaces to/from the PNet, port A, and port B to various circuits in the core logic, reset, and halt interface. The IRQ ports are not used. The right side of the CPU contains address and data lines and chip select outputs. The 68302 operates with a statically defined 8-bit wide bus. The following resources are used for specific Module functions:

CHIP SELECTS LOGIC

CS0-0	FLASH ROM
CS1-0	STATIC RAM
CS2-0	ADC SELECT
CS3-0	PNEUMATIC CONTROLS

SERIAL COMM CHANNELS

SCC1	PNET [RXD1, TXD1, RCLK1, TCLK1, CTS1-0, RTS1-0]
SCC2	ASYNC DEBUG [RXD2,TXD2]
SCP	SERIAL EEPROM [SPRXD,SPTXD,SPCLK]
TIMER1	SYSTEM TIMEBASE

PARALLEL IO / SPECIAL PURPOSE IO BITS

PA2	CHIP SELECT TO SERIAL EEPROM
PA5	ASYCN_EN (PNET MODE SELECT)
PA6	POWER MANAGEMENT CONTROL
PB5 /TIN2	TIMEBASE INPUT FOR EXTERNAL MEMORY / SYSTEM CONFIG
PB7	WATCHDOG TIMER OUTPUT

Program Memory. Program memory consists of 8-bit flash ROM U11 shown on sheet 5 of the schematic. The ROM is configured for 128Kx8 (1024k bit). The ROM is not socketed and cannot be removed for programming. The ROM can be flash-programmed via the logic analyzer interface or the PNET connector.

Data Memory. Data is stored in 128Kx8 static RAM U3. This RAM is cleared when power is removed.

Non-volatile Memory. Serial EEPROM U1 is a 128-byte PROM that provides non-volatile storage for model and serial number information and parameter user interface data which must travel with the Module. The 68302 synchronous communication port (SCP) is used to access the EEPROM.

Logic Analyzer/Test Interface. The logic analyzer/test interface is shown on sheet 6 of the schematic. The core logic includes an interface to bring signals required for external ROM access, logic analyzer interface, and a debug serial channel to a single connector.

The external ROM access allows an off board ROM (8 bit) or ROMs (16 bit) to replace the FLASH devices at address 0. Address, data, and control signals required for this function are included on the LA/T connector.

All signals needed for a Hewlett Packard model 16500 logic analyzer or equivalent to perform bus state analysis and disassembly are included on the LA/T connector.

The 68302 SCC2 serial transmit and receive data signals are included on the LA/T connector.

The LA/T connector pinouts are as follows:

PIN	NAME	PIN	NAME
1,69	+5V	2,28,45,46,70	GND
3	A0	4	A1
5	A2	6	A3
7	A4	8	A5
9	A6	10	A7
11	A8	12	A9
13	A10	14	A11
15	A12	16	A13
17	A14	18	A15
19	A16	20	A17
21	A18	22	A19
23	A20	24	A21
25	A22	26	A23
29	D0	30	D1
31	D2	32	D3
33	D4	34	D5
35	D6	36	D7
37	D8	38	D9
39	D10	40	D11
41	D12	42	D13
43	D14	44	D15
47	DTACK-0	48	AS-0
49	RW	50	UDS-0
51	DS-0	52	BGACK-0
53	FC0	54	FC1
55	FC2	56	DEBUG TXD
57	DEBUGRXD	58	EXROMCS-0
63	PRGM_EN	64	DISCPU
65	T1_IN		

DISASSEMBLY PROCEDURE

STATIC DISCHARGE CAUTION

Do not attempt to service unit without static discharge protection. Workstations and personnel must be properly grounded, or damage to equipment will result.

1. Remove two 4-40 x 5-1/8" screws from the rear of the Module. Remove rear cover.

2. Turn Module upside down (to facilitate removal of the enclosure). Carefully slide the enclosure away from the front panel, keeping the PWAs and front panel together.

3. Turn Module upright. Unsnap two tabs at top of assembly, and remove card guide.

4. Carefully disconnect the flex cable of transducer bracket (15, FO-42B) from J103 of the analog PWA.

5. Pull front panel away from the hose of the pump assembly.

6. Carefully separate and unplug digital PWA from analog PWA.

7. Disconnect the flex cable from J105 of the analog PWA.

8. Disconnect cable from J102 of analog PWA, and separate analog PWA from pump assembly

9. Using FO-42B as a guide, perform any additional disassembly that may be required for maintenance procedures.

REASSEMBLY PROCEDURE

1. If disassembled, prepare pneumatic manifold and pump assembly (5) and hose (21) as shown in FO-42B.

2. Attach analog PWA (7) by aligning manifold standoff with grommet of PWA and aligning edge of PWA with pump assembly shock mount.

3. As shown in FO-42B, connect cable to J102 of analog PWA and connect flex cable to J105.

4. Attach digital PWA (8) by aligning interface connector pins and by aligning manifold standoff with grommet of PWA, and carefully press PWAs together.

5. Seat pump assembly hose onto barb fitting of front panel assembly.

6. If disassembled, reassemble front panel components as shown in FO-42B. Connect flex cable from transducer (15) to J103 of analog PWA. Rotate front panel assembly to facilitate connection of cable.

7. Push card guide (6) onto slots of assembled PWAs.

8. With enclosure oriented so large groove is at bottom and label is at right (viewed from front of Module), slide enclosure over front cover and attached PWA assembly

9. Install back cover on the Module enclosure.

10. Fasten the front and rear covers to the enclosure by inserting two 4-40 x 5-1/8" screws from the rear through the enclosure to the front cover as shown in FO-42B. Tighten the two screws to 4-in/lb.

PARTS LISTS

NIBP Module parts lists and location drawings are organized as follows:

Item	Parts List	Drawing
Top Assembly 7300	Table 42-11	FO-42B
NIBP Analog PWA 315-452	Table 42-12	FO-42C
NIBP Digital PWA 315-459	Table 42-13	FO-42D
Pneumatic Manifold Assembly 320-646	Table 42-14	FO-42E

Table 42-11. Top Assembly 7300 Parts List

Item	Description	Part No.
3	SCREW, 2-56X3/16 PNH PHH SST	719-237
4	PWA, FLEX, CUFF PRESSURE, NIBP	313-114
5	PNEUMATIC MANIFOLD ASSY, SINGLE-WIDE	320-646
6	INSULATION, GUIDE, MODULE	750-182
7	PWA, NIBP ANALOG	315-452
8	PWA, NIBP DIGITAL	315-459
9	PANEL, FRONT NIBP/TEMP SINGLE WIDE	701-415
10	COVER, PARAMETER REAR	703-188
11	SUB-ASSY, ENCLOSURE, EXTRUDED SW	320-676
15	BRACKET, TRANSDUCER	704-932
17	SCREW, RDH PHH, 4-40X51/8, CUSTOM	722-201
18	BUTTON, LATCH, SW	732-166
19	SPRING, CONTACT, GROUND	736-204
20	O-RING, .55 ID X .070 SILICONE	752-245
21	TUBING PHARMED	740-185
22	GROMMET, DAMPING	752-246
23	SCREW, 4-40X1/4 PNH PHH SST	719-102
24	HOSE BARB, 0.125 ID TUBING, BRASS	712-257
29	SCREW, 4-40X3/16 PNH PHH SST	719-101
31	STANDOFF, 15/16 INCH	735-314
32	GASKET, FRONT PANEL NIBP	752-276

Table 42-12. NIBP Analog PWA 315-452 Parts List

Item	Description	Part No.
C2-19,21-31, 33,44-53,55, 56	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
C35, 36	CAP,METAL POLYESTER, 1.0 UF 5%, 40V SMD	603-221
C37	CAP,2917/DTANT,16V,20%,22UF	606-110
C38-39	CAP,CERAMIC,SMD,X7R,50V,1.0 UF	605-361
CR1-5	DIO SWI, 200 MA, 70V, SMD	610-114
CR6	DIODE 1AMP, 50V GEN PUR SMT	610-123
D1	DIO, ZENER 12.0V, 5%, .5W SUR MOUNT	612-133
J1	CONN,HEADER,2POSN,2MM,.02SQ,R ANGL,SMT	607-894
J100	CONN, FLEX CABLE, 30 PIN 0.05 PITCH, STR	608-285
J102	CONNECTOR, 6 PIN DUAL ROW	607-826
J103-105	CONN, HEADER 6 PIN, 1.25MM STRAIGHT, SMT	607-890
Q4	XSTR, N-CHAN MOS SOT-23	676-130
R1	RES, WW, 0.1 OHM, 1%, 1W, SMT	655-132
R2	RES,SMD,1/10W,1%,10.0 OHM	685-101
R32-38,54,82, 84	RES,0603,1/16W,1%,10.0K OHM	686-389
R45	RES,0603,1/16W,1%,16.9K OHM	686-411
U1	IC, LATCH SUR. MT.	692-112
U2	IC, PRECISION 5V REFERENCE	693-161
U3,6,10,12,17	IC, DUAL OP-AMP FET SOIC	691-139
U4,7	IC, AD620BR, INSTRUMENTATION AMP, SMT	692-187
U5,8,13	IC, DUAL JFET OP AMP SOIC	691-110
U9	IC, DG508A ANALOG MUX, CMOS SOW-16	693-109
U11	IC, CMOS DIGITALLY CONTROLLED POT, SMT	692-208
U14	IC, QUAD COMPARATOR, PRECISION	691-128
U15	IC, QUAD SPST ANALOG SWITCH SUR MT	693-112
U16	IC, PLD, CMOS, 22V10, 24PIN SOIC	692-241

Table 42-13. NIBP Digital PWA 315-459 Parts List

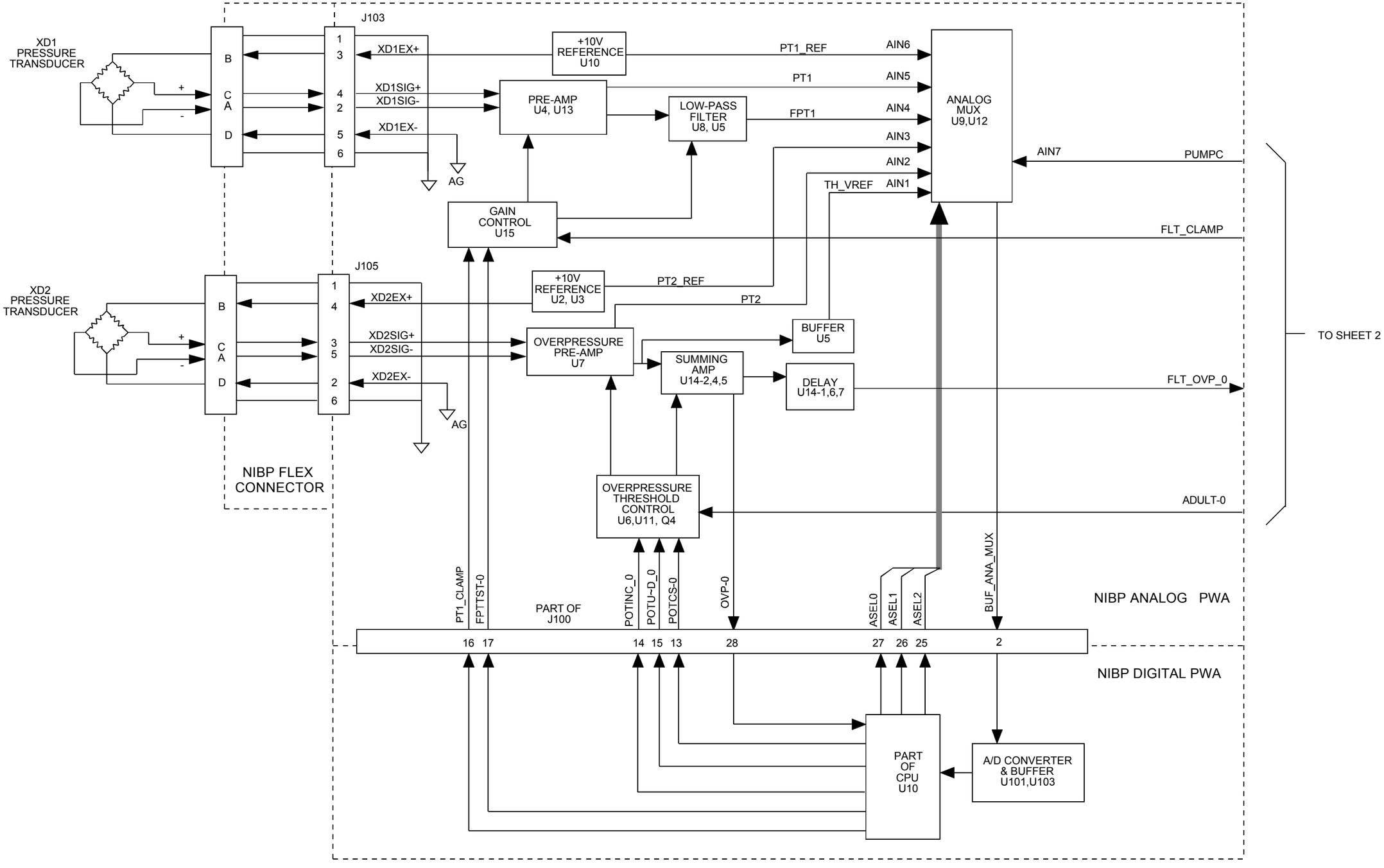
Item	Description	Part No.
C2,3	CAP,CER,SMD,0603,NPO,10%,50V,27 PF	605-718
C4-14,16,102, 104,106108, 113,114	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
C101,103,105 ,109	CAP,2917/D,TANT,35V,20%,10 UF	606-188
C112	CAP,2917/D,TANT,35V,20%,4.7UF	606-186
C115	CAP,CERAMIC,SMD,X7R,50V MIN,1000 PF	605-209
CR1,13	DIODE, SCHOTTKY, 30V, 200MW, SOT-23	611-137
CR2-7,10,11	DIODE, DUAL SERIES SMT SOT-23	611-140
CR12	DIO ZENER 6.2V, 5% SMT, 225MW	612-147
FB1-FB9	FERRITE CHIP, EMI SUPPRESSION, SMT	669-170
J1	CONN, 20 PIN PLUG RT ANGLE PC MOUNT	607-795
J4	SOCKET, MICRO STRIP 35X2, SMD	607-816
J100	CONN, 30 PIN, 050 PITCH, SIP HDR	607-839
J101	CONN, HEADER 6 PIN 1.25MM, R-ANGLE, SMT	607-889
Q1	XST NPN 2222A SMT	674-127
Q100	XSTR, MOSFET, P-CHAN, 4A, 30V, SMT	676-162
Q101,103	XSTR, N-CHAN MOS SOT-23	676-130
Q102	XSTR, MOSFET, P-CHAN, .12A, 60V, SOT-23	676-161
R1,40,41,44, 50	RES,0603,1/16W,1%,1.00K OHM	686-293
R2	RES,0603,1/16W,1%,4.99K OHM	686-360
R3,4,7-33,35, 42,43,47,48, 102,128-130, 132,135,137	RES,0603,1/16W,1%,10.0K OHM	686-389
R5,6	RES,0603,1/16W,1%,2.21K OHM	686-326
R34	RES,0603,1/16W,1%,698K OHM	686-566
R45	RES,0603,1/16W,1%,100 OHM	686-197
R46	RES,0603,1/16W,1%,47.5K OHM	686-454
R100,101, 104-121	RES,0603,1/16W,1%,499 OHM	686-264
R131	RES, WW, 100 OHMS, 1%, 1W, SMT	655-133
R133,134,136	RES,SMD,1/10W,1%,10.0 OHM	685-101
U1	IC,93C56 2KBIT SERIAL EEPROM,CMOS SM	692-183
U2	IC, EECMOS PLD 16V8B, ARRAY LOGIC	692-226
U3	IC, 128X8 70NS CMOS SRAM TSOP	694-133
U4	IC,74AC32 QUAD 2 IN OR GATE,ADV CMOS SM	692-141

Table 42-13. NIBP Digital PWA 315-459 Parts List (Continued)

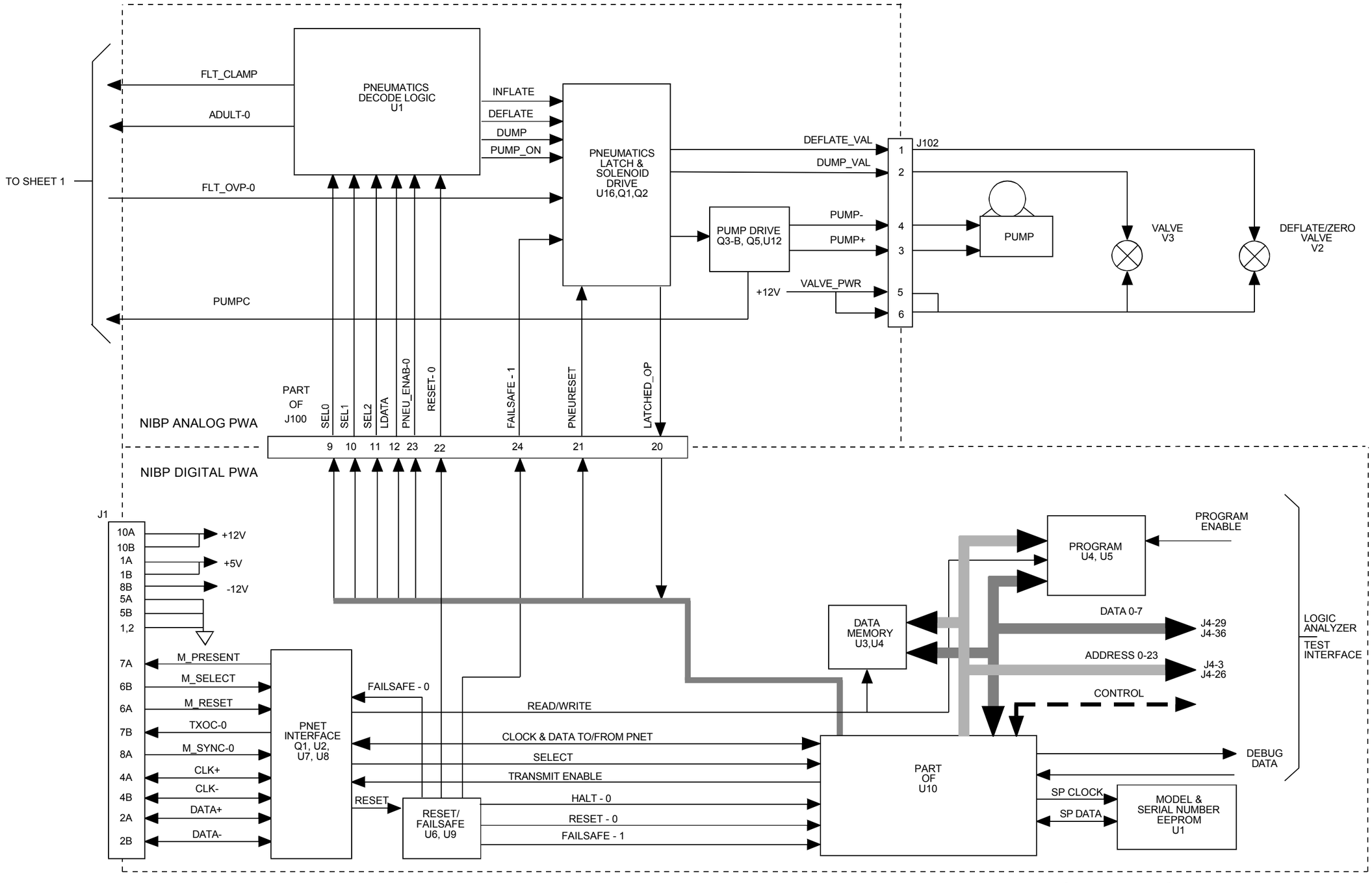
Item	Description	Part No.
U5	IC, 128K X 8-BIT 5V FLASH ROM CMOS SMT	692-195
U6	IC,74HC03 QUAD 2 IN.NAND,CMOS SUF MT	692-139
U7,8	IC, CMOS LTC1485, DIFF BUS XCEIVER SO8	692-225
U9	IC, POWER SUPPLY MONT WITH RESET SMT	694-118
U10	IC, 68302 MICROPROC., 20MHZ SMT	694-136
U101	IC, CMOS MAX 163 12BIT ADC, SMT	692-233
U102	IC, DRIVER/RECEIVER, SMT	692-242
Y100	CRYSTAL, 19.5104 MHZ, 0.005% HC-49UP	609-136
#64	PAL_U2A, CORE LOGIC	637-101

Table 42-14. Pneumatic Manifold Assembly 320-646 Parts List

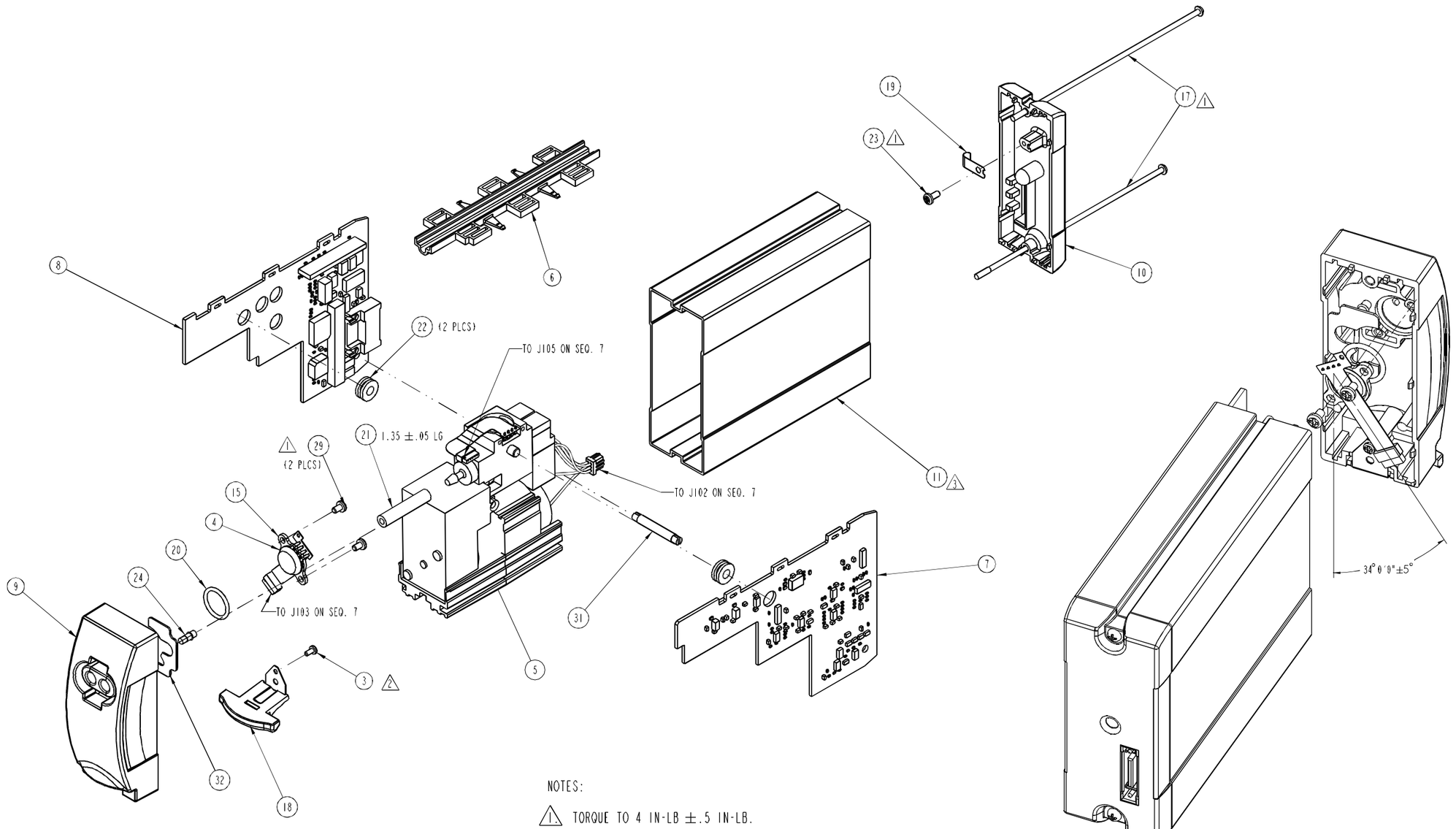
Item	Description	Part No.
1	PUMP, ROTARY PISTON 12VDC MOTOR	712-253
2	MANIFOLD INSEPARABLE ASSY, SINGLE WIDE	320-681
3	O-RING, .176 ID X .040	752-243
4	FILTER NOMINAL, 0.343 IN DIA, 40 MICRON	754-142
5	VALVE, CHK, CARTRIDGE, 3IN WATER	754-150
6	VALVE, SOLENOID 12VDC, 0.045 IN, 1/2W	754-154
7	O-RING	752-275
8	SLEEVE, PUMP	759-323
9	O-RING, .55 ID X .070 SILICONE	752-245
10	O-RING .489 ID X .070	752-232
12	SCREW, 4-40X1/4 PNH PHH SST	719-102
13	TAPE, TEFLON 1/4 INCH WIDE, WHITE	774-167
14	RETAINER, TRANSDUCER	736-209
19	FITTING HOSE 1/8 NPS	712-266
20	PLUG, BOTTOM, LARGE	752-274
21	PIN, GROMMET	752-273
23	SCREW, 4-40X1/4, FLH, PHH, 100 DEG, SST	719-305
26	CRADLE, PUMP, MOLDED	704-877
28	PWA, FLEX, OVER PRESSURE, NIBP	313-113
29	CONNECTOR, 6 PIN	607-863
30	FILTER NOMINAL, 0.410 IN DIA, 40 MICRON	754-151
31	FILTER NOMINAL, 0.155 IN DIA, 40 MICRON	754-152
32	FITTING MODIFIED	712-267



FO-42A. NIBP Singlewide Module Block Diagram (1 of 2)



FO-42A. NIBP Singlewide Module Block Diagram (2 of 2)



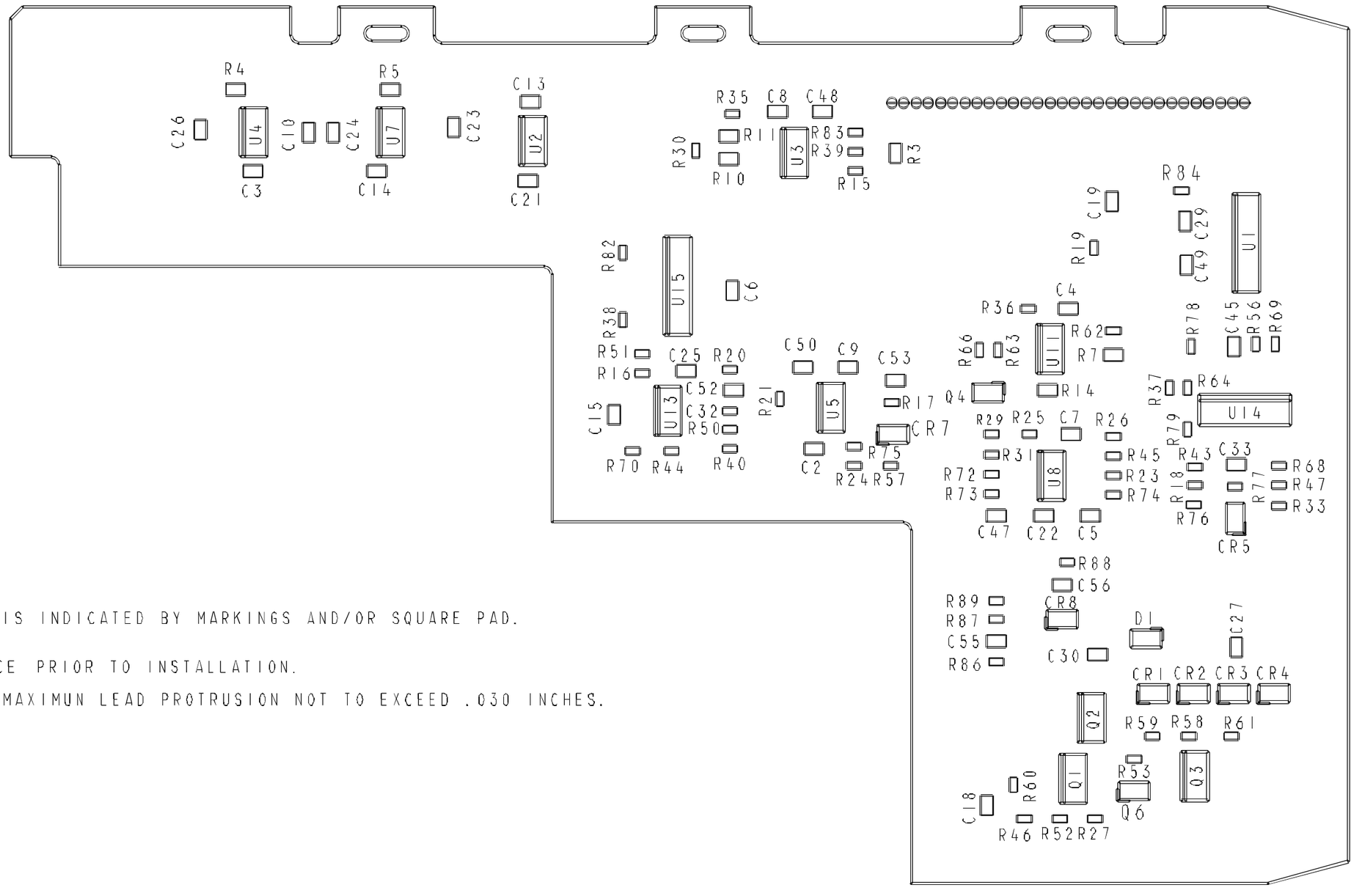
NOTES:

1. TORQUE TO 4 IN-LB ±.5 IN-LB.
2. TORQUE TO 3 IN-LB ±.5 IN-LB.
3. ENCLOSURE TO BE ORIENTED WITH SMALLER GUIDE GROOVE AT TOP.

FO-42B. Top Assembly 7300

SIDE 1 - PRIMARY

(OUTSIDE)



NOTES:

3. PIN NUMBER 1 IS INDICATED BY MARKINGS AND/OR SQUARE PAD.

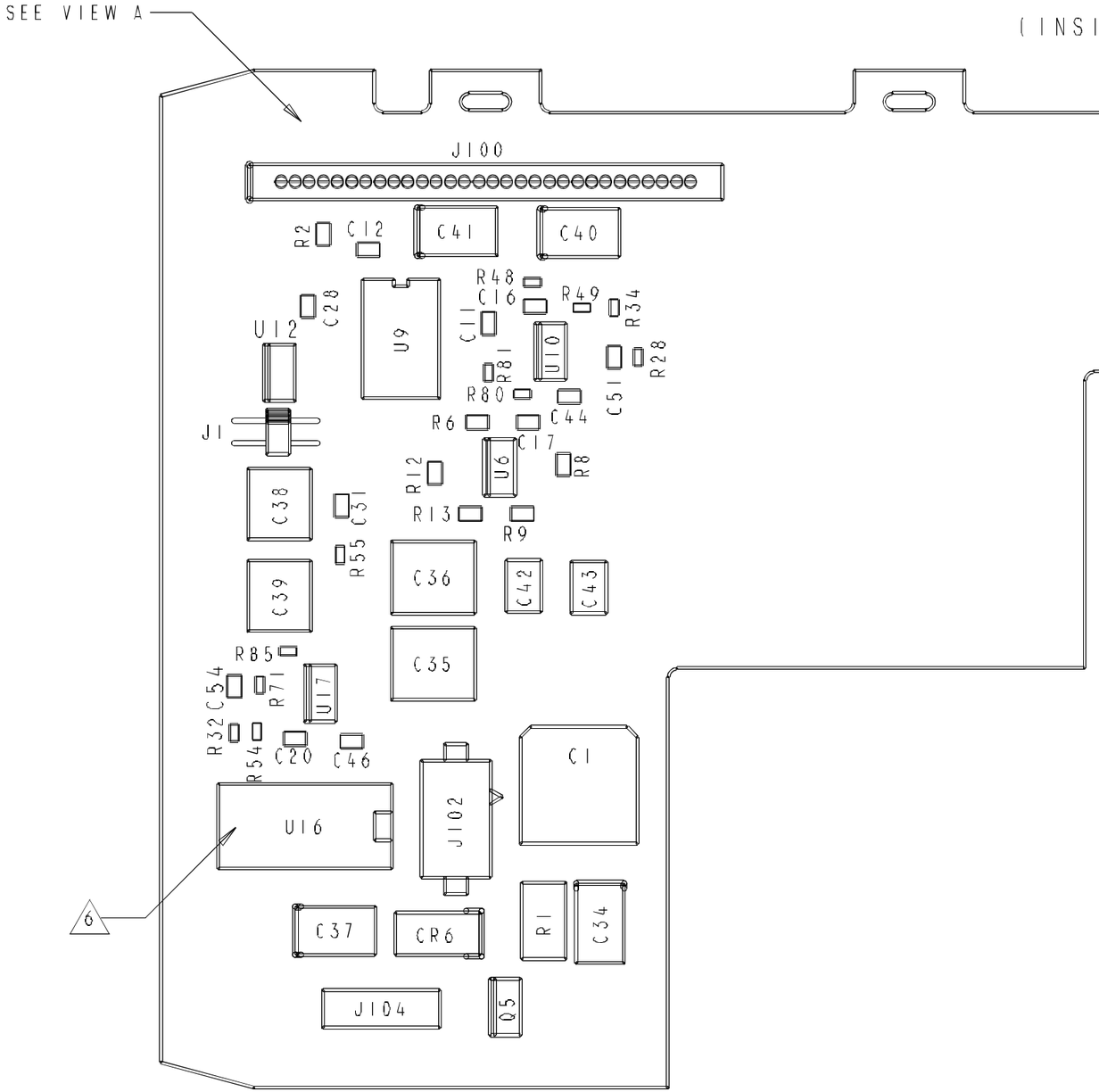
6. PROGRAM DEVICE PRIOR TO INSTALLATION.

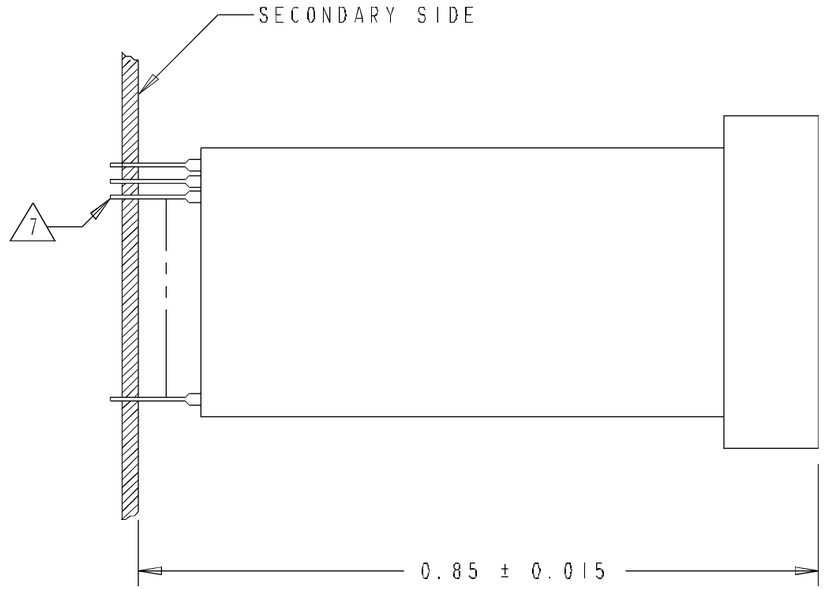
7. PRIMARY SIDE MAXIMUN LEAD PROTRUSION NOT TO EXCEED .030 INCHES.

FO-42C. NIBP Analog PWA 315-452 (1 of 2)

SIDE 2 - SECONDARY

(INSIDE)

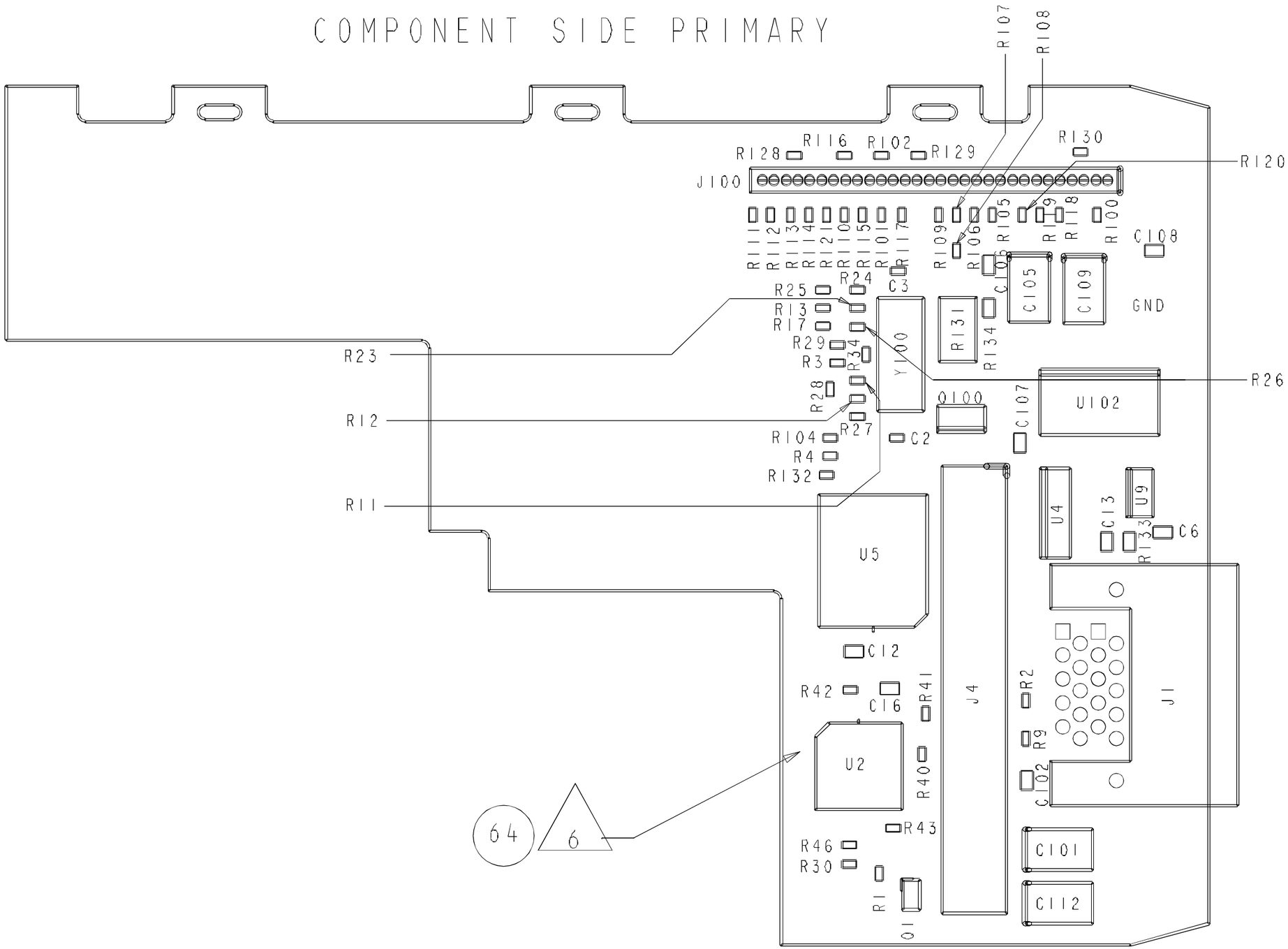




VIEW A

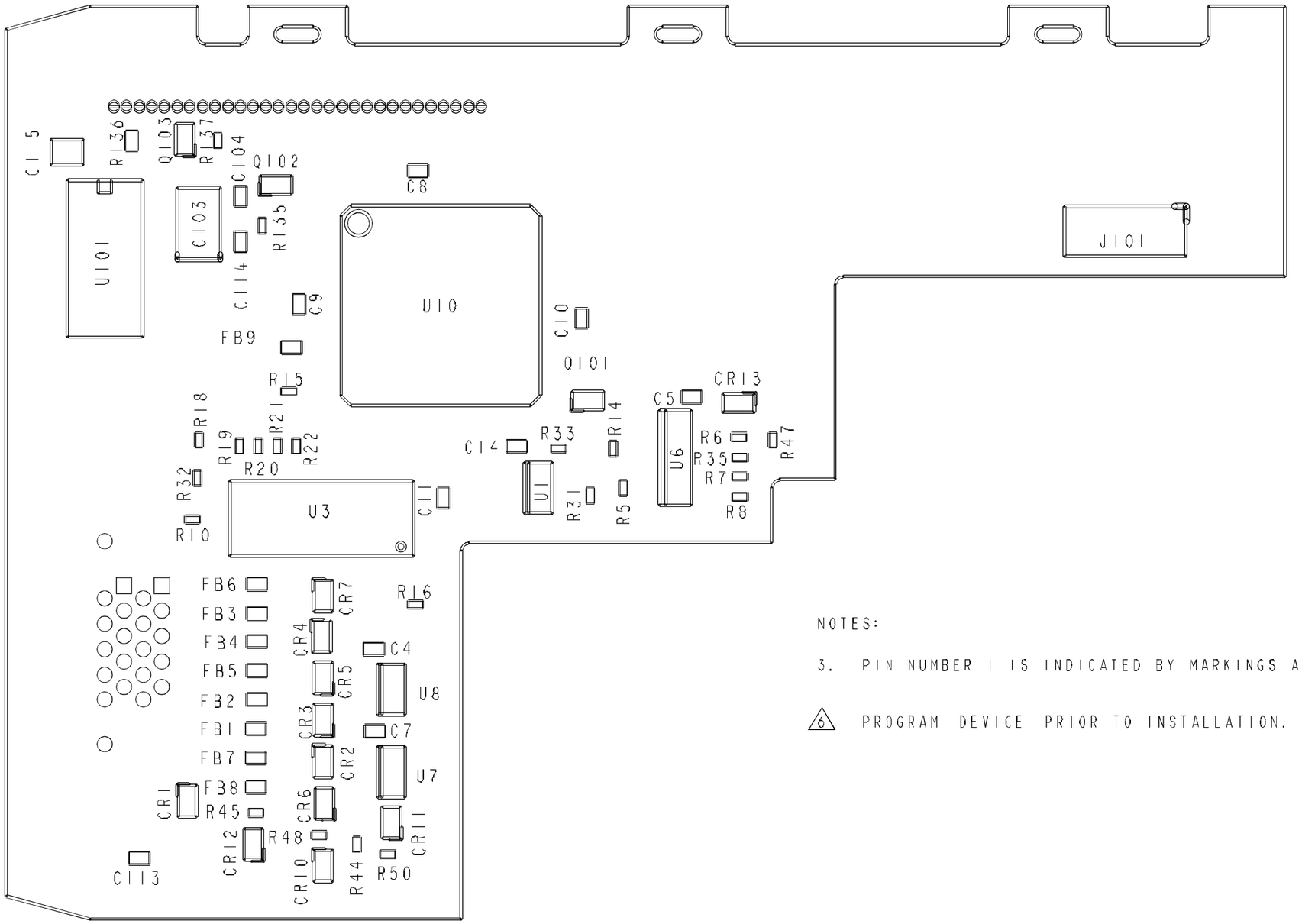
SCALE=NONE

FO-42C. NIBP Analog PWA 315-452 (2 of 2)



FO-42D. NIBP Digital PWA 315-459 (1 of 2)

COMPONENT SIDE SECONDARY

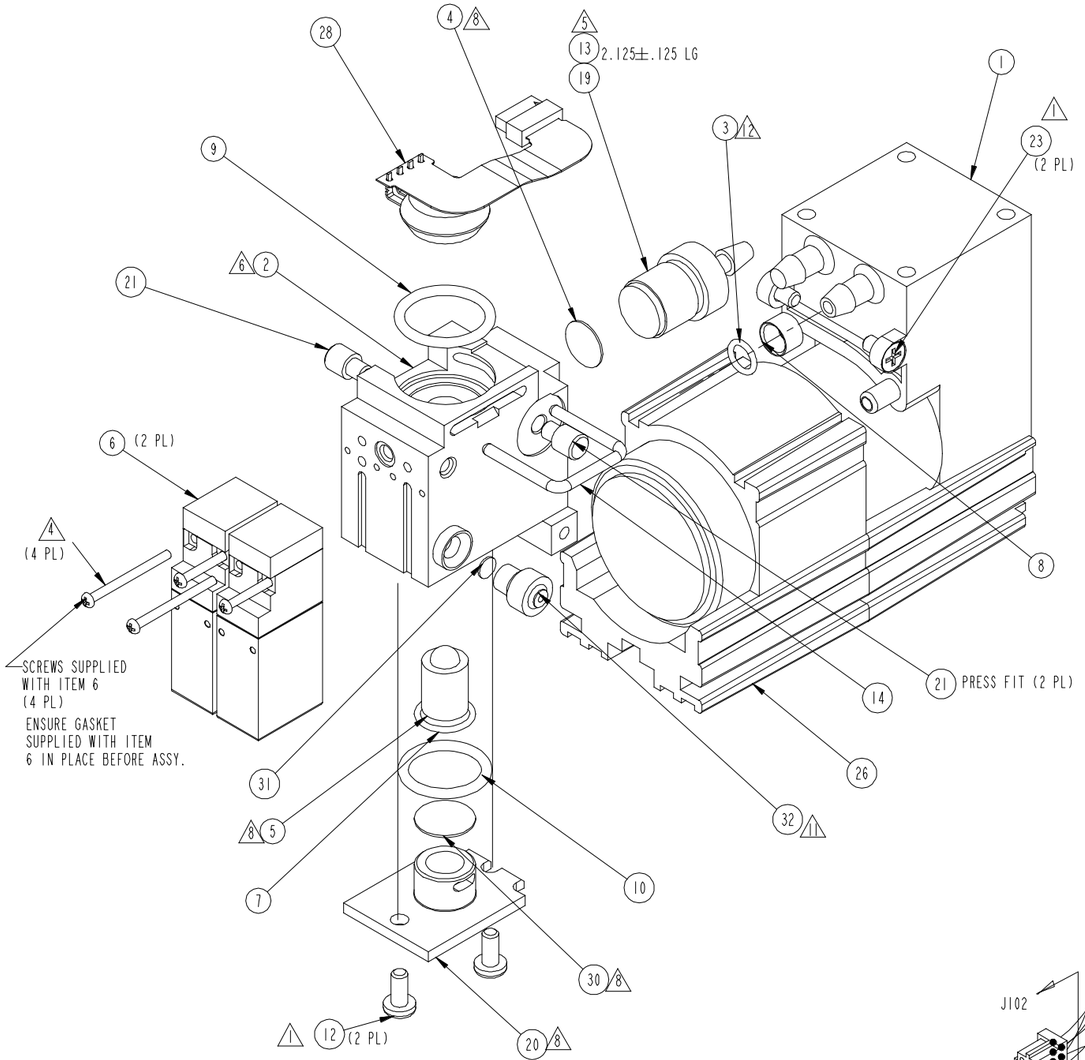


NOTES:

3. PIN NUMBER 1 IS INDICATED BY MARKINGS AND/OR SQUARE PAD.

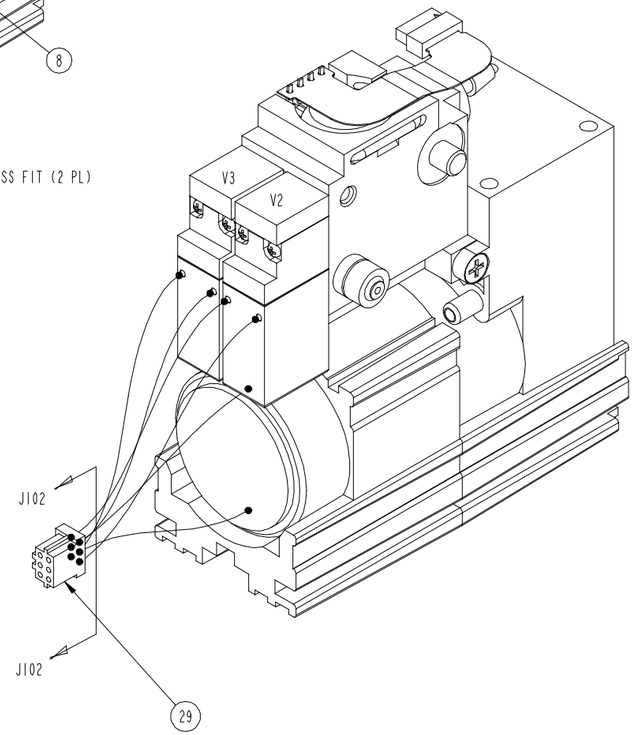
⚠6 PROGRAM DEVICE PRIOR TO INSTALLATION.

FO-42D. NIBP Digital PWA 315-459 (2 of 2)



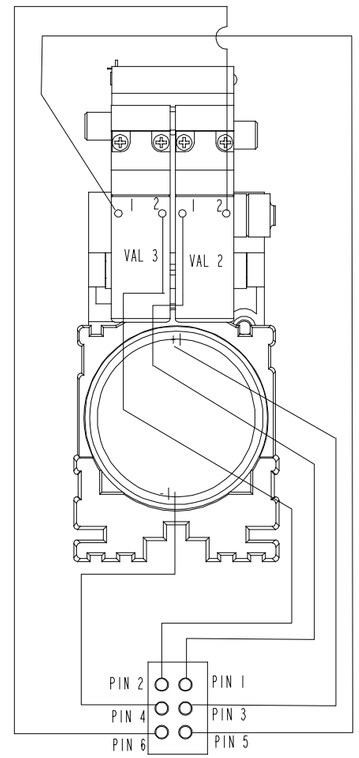
NOTES:

1. TORQUE TO 4 IN-LB ±1 IN-LB
2. TORQUE TO 8 IN-LB ±1 IN-LB
4. TORQUE 4 SCREWS TO 6 IN-OZ THEN RETORQUE TO 10 IN-OZ ±1 IN-OZ.
5. TORQUE TO 11 ±1 IN-LB.
6. ITEM 2 TO BE FREE OF DEBRIS AND/OR MACHINING OILS PRIOR TO ASSEMBLY.
7. ENERGIZE EITHER VALVE (ITEM 6) BEFORE ENERGIZING PUMP (ITEM 1) MOTOR.
8. ULTRASONICALLY CLEAN WITH REAGENT GRADE ALCOHOL
11. TORQUE TO 2 IN-LB ±.5 IN-LB
12. APPLY RUBBER LUBRICANT TO O-RING AS REQUIRED.



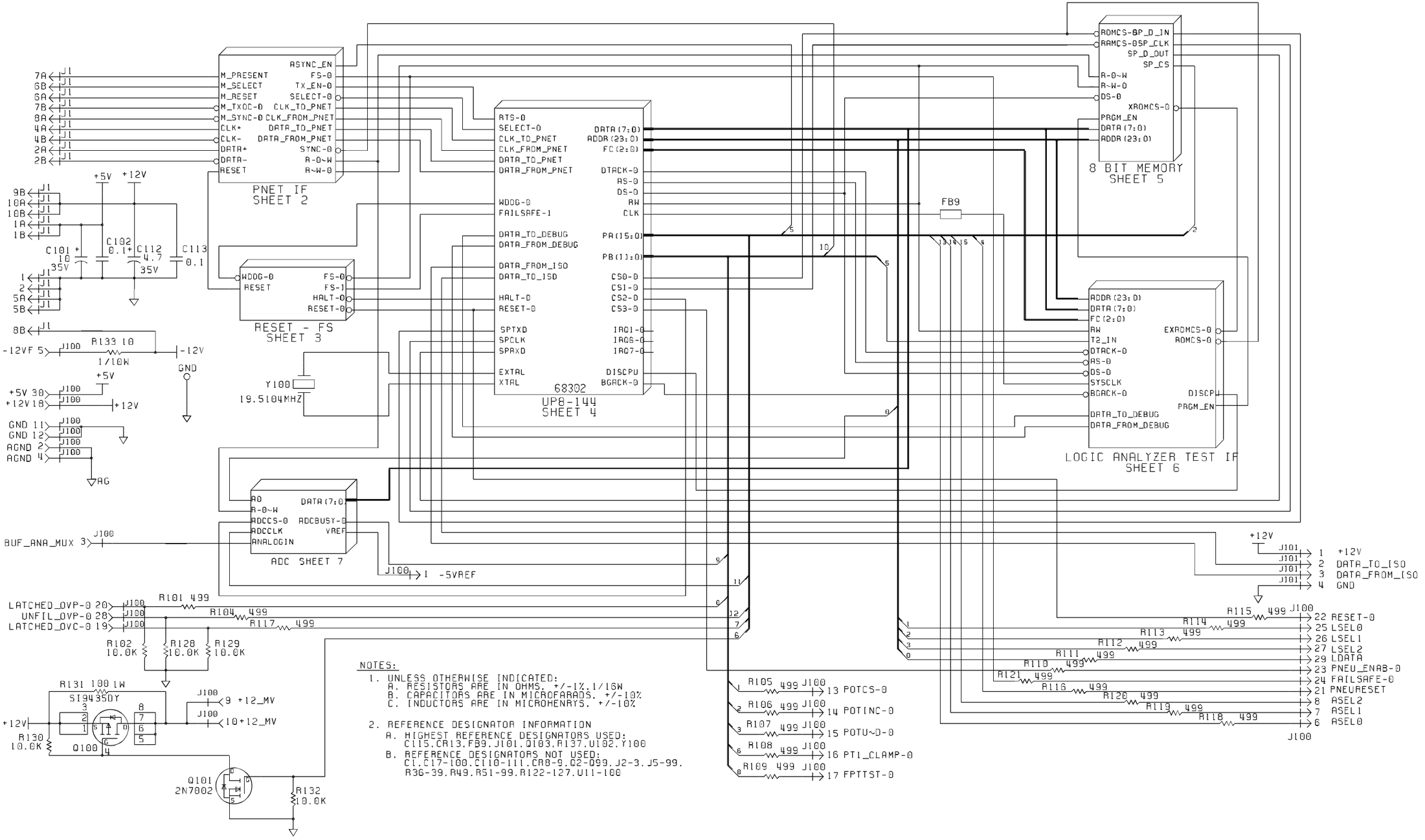
(SEE CONFIGURATION CHART)

CONFIGURATION CHART	
FROM	TO
J102-1	VAL 2 - PIN 1
J102-2	VAL 3 - PIN 2
J102-3	PUMP (+)
J102-4	PUMP (-)
J102-5	VAL 3 - PIN 1
J102-6	VAL 2 - PIN 2

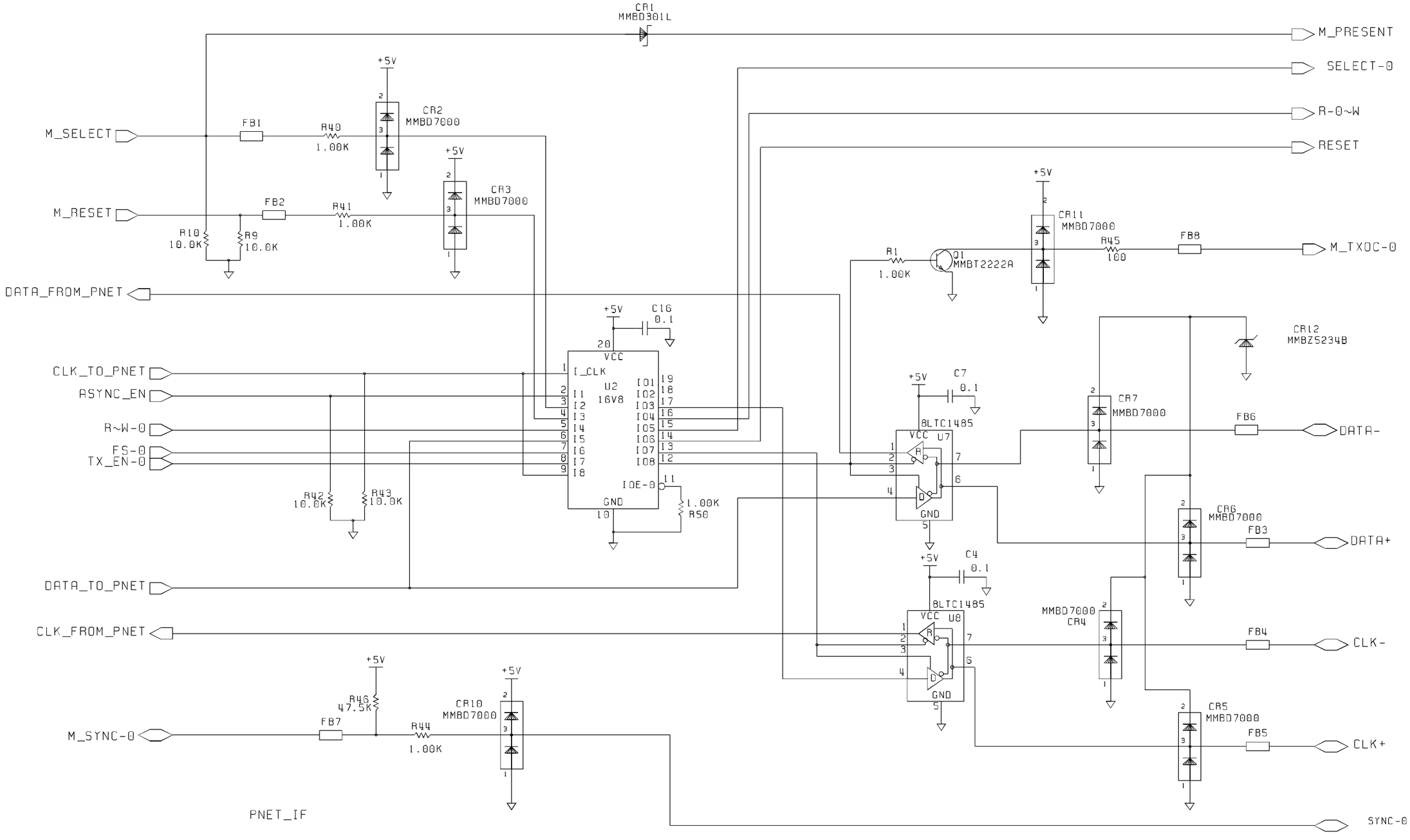


VIEW J102

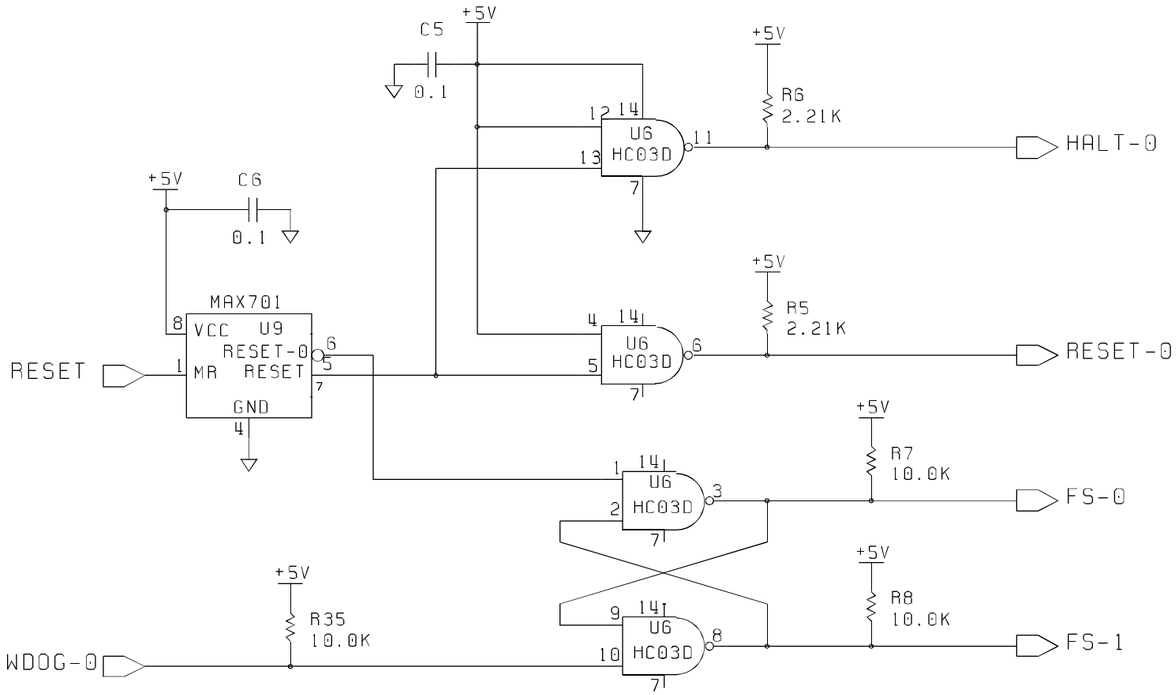
FO-42E. Pneumatic Manifold Assembly 320-646



SC315-459 A
NIBP Digital PWA Schematic (1 of 7)

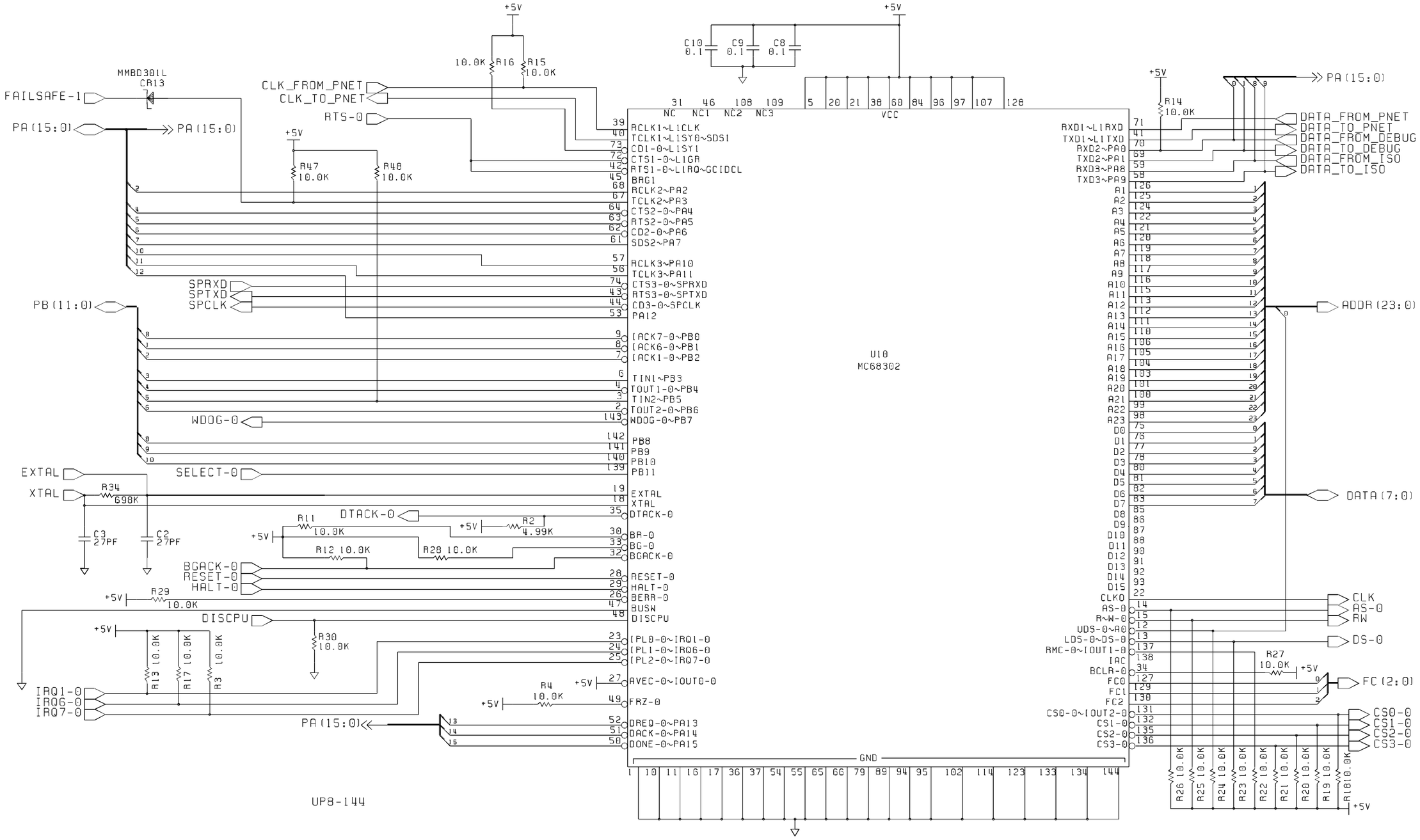


SC315-459 A
NIBP Digital PWA Schematic (2 of 7)

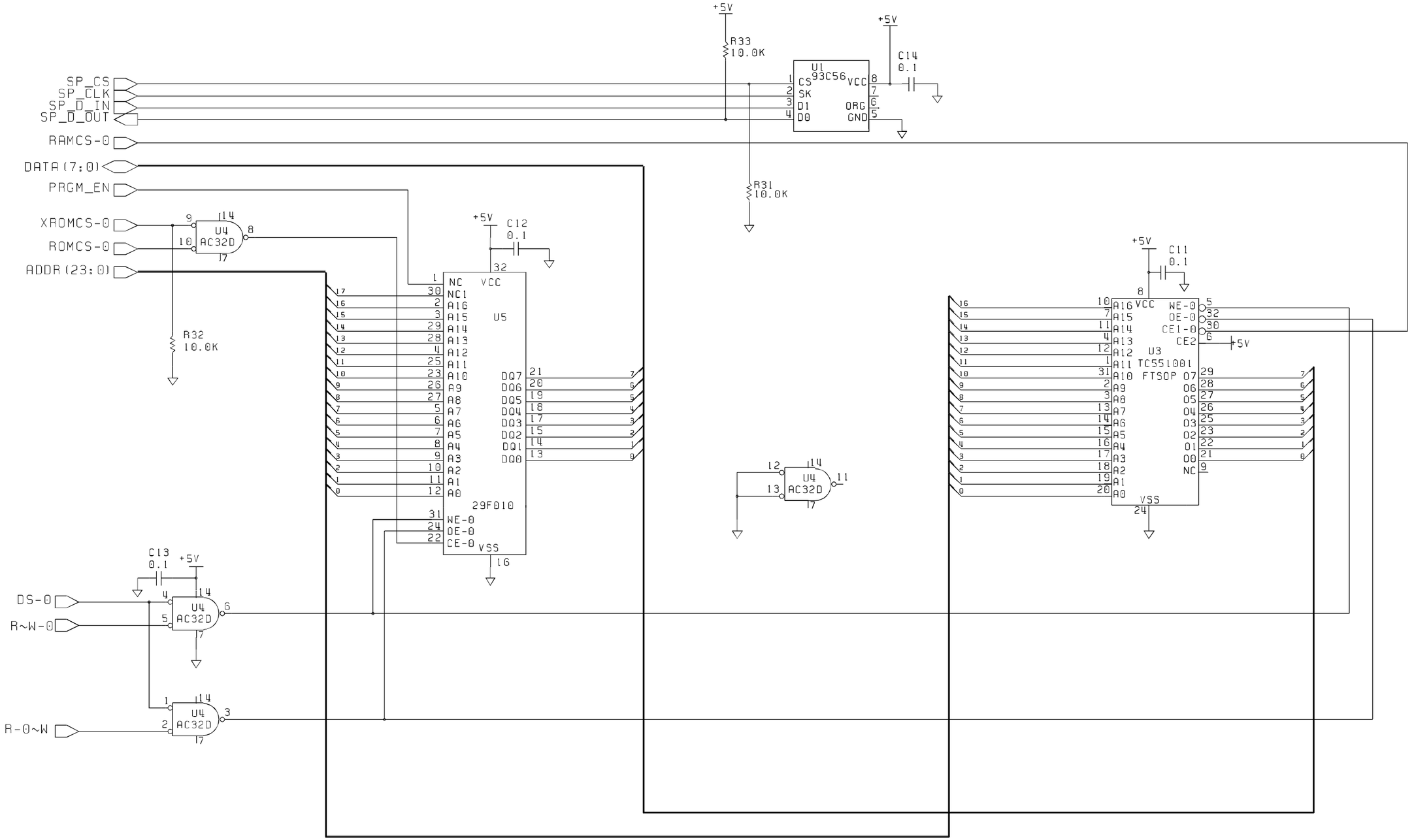


RESET - FS

SC315-459 A
NIBP Digital PWA Schematic (3 of 7)

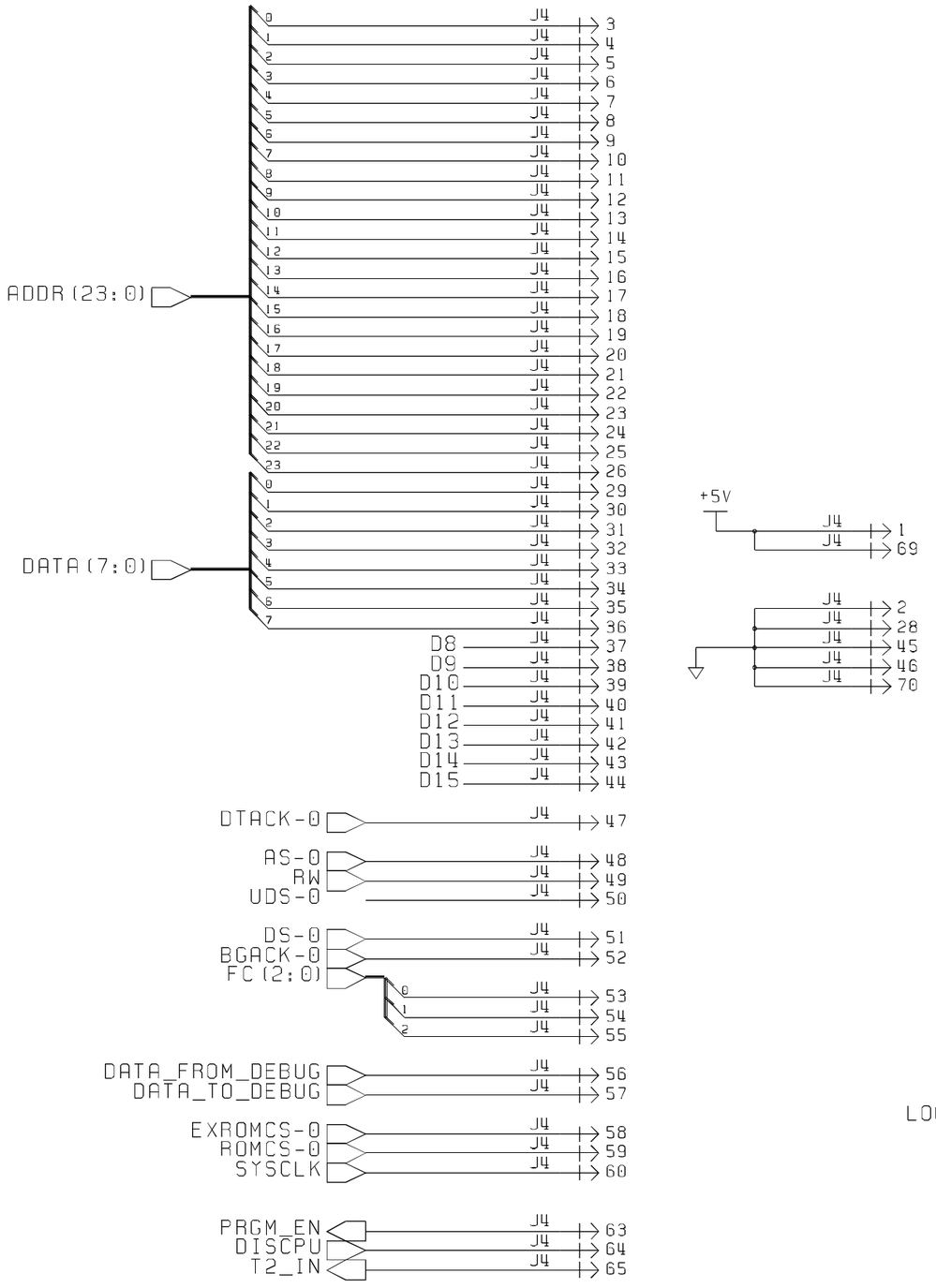


SC315-459 A
NIBP Digital PWA Schematic (4 of 7)



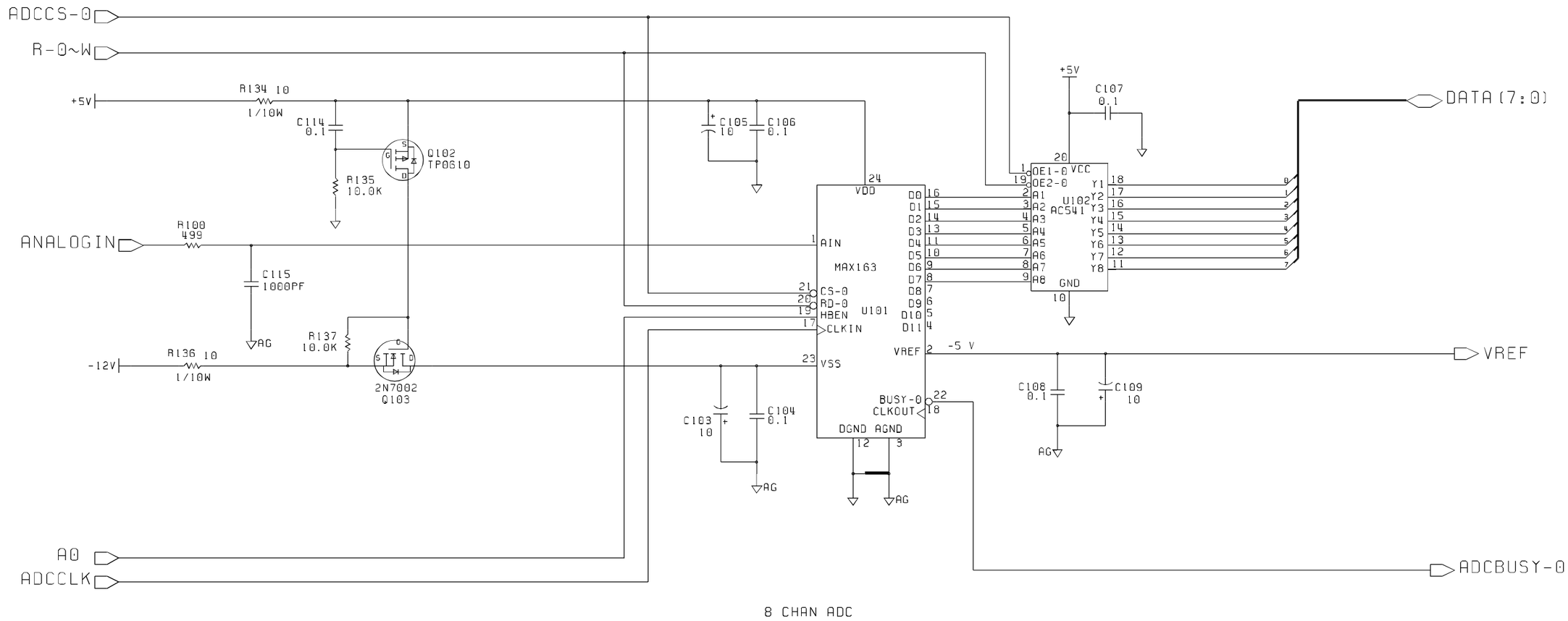
8 BIT MEMORY_2

SC315-459 A
NIBP Digital PWA Schematic (5 of 7)



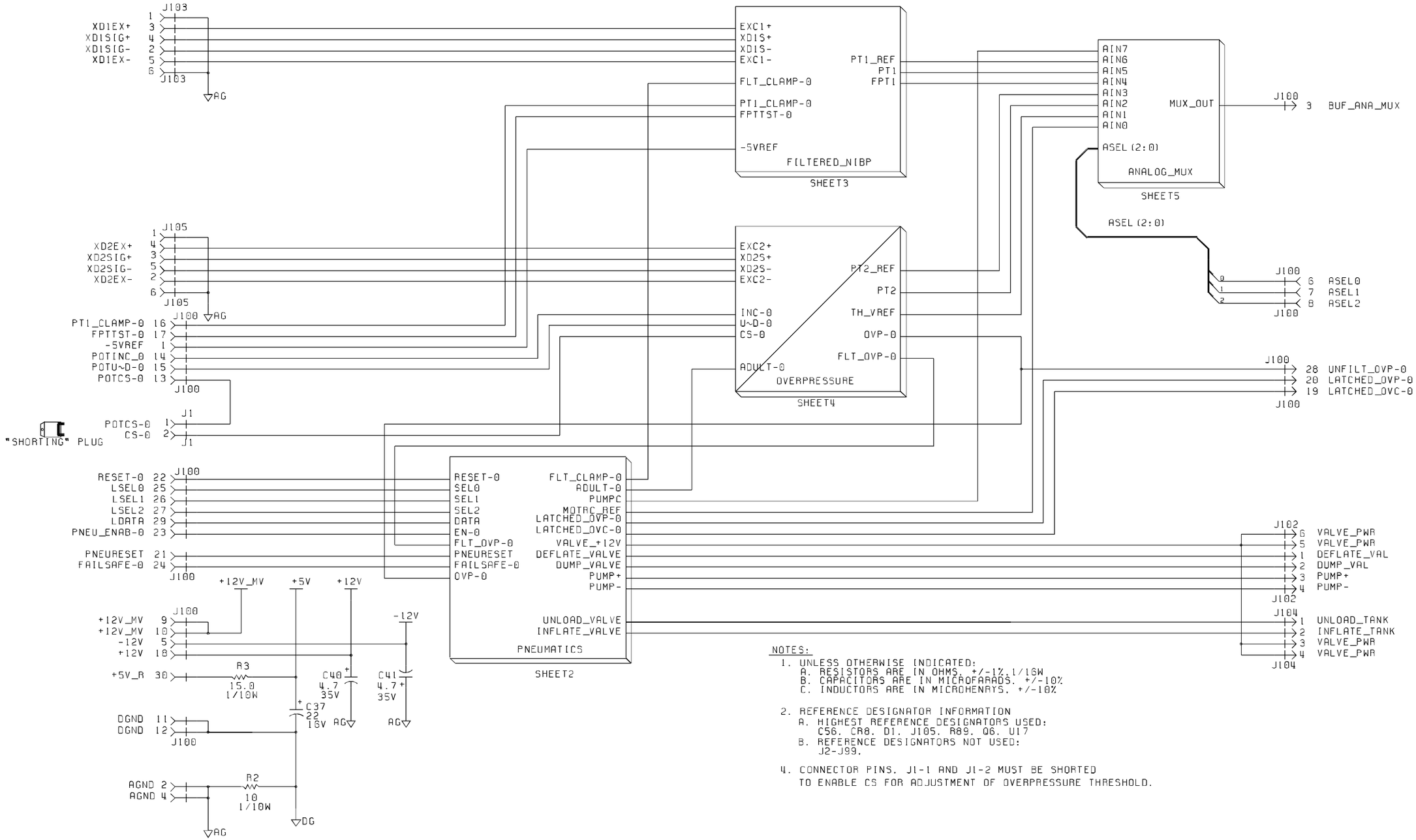
LOGIC ANALYZER TEST IF_4

SC315-459 A
NIBP Digital PWA Schematic (6 of 7)

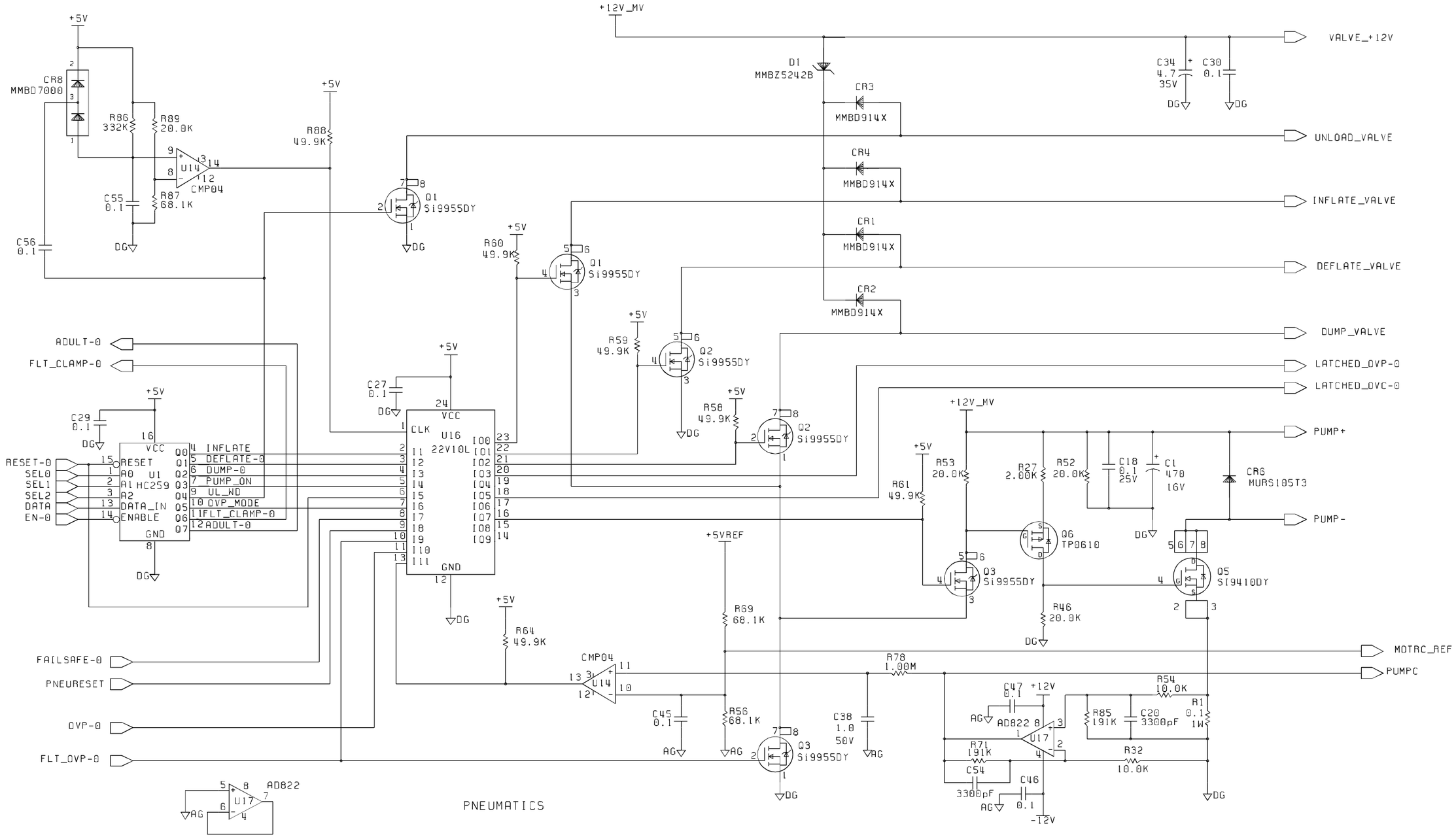


8 CHAN ADC

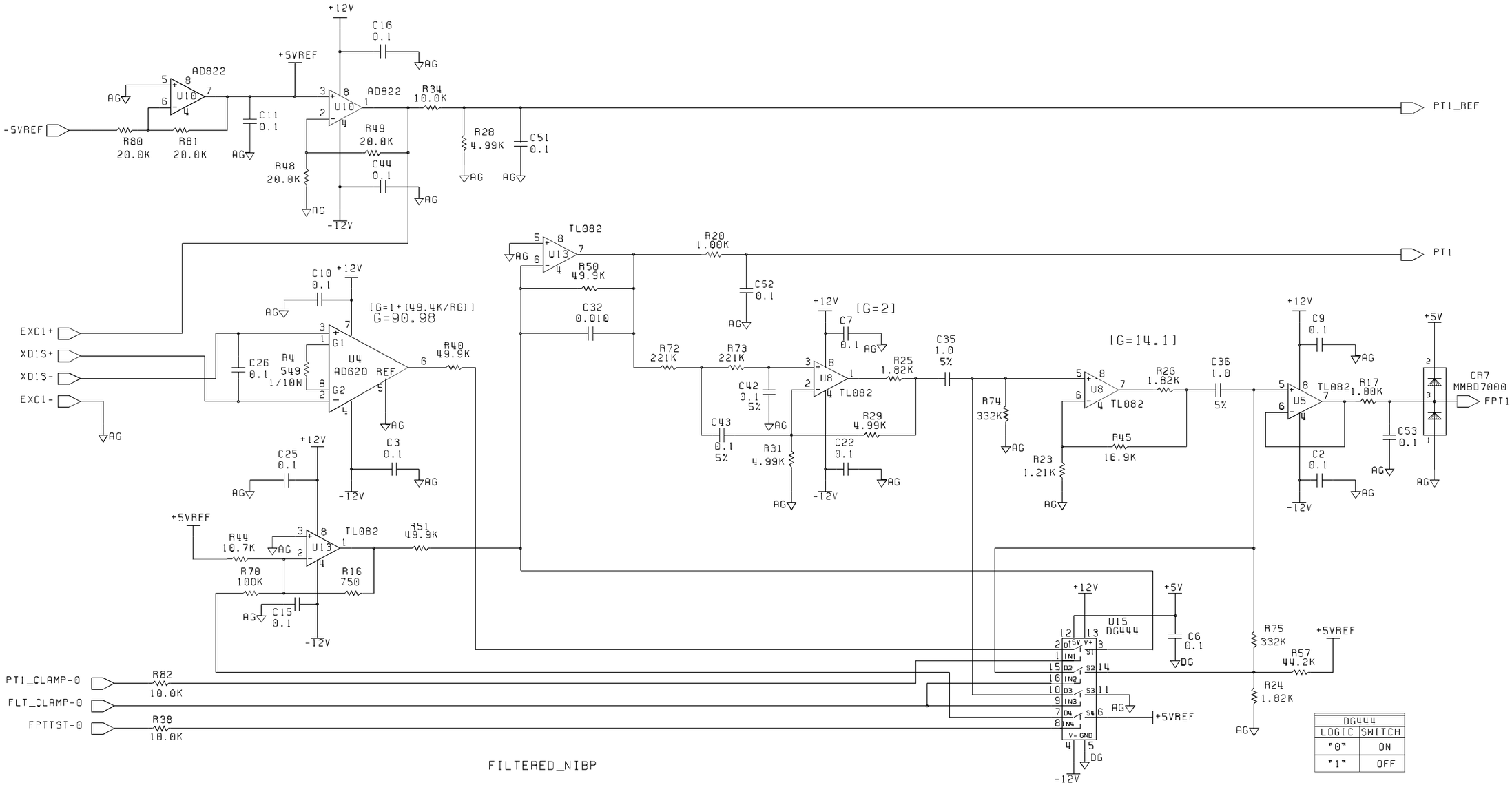
SC315-459 A
NIBP Digital PWA Schematic (7 of 7)



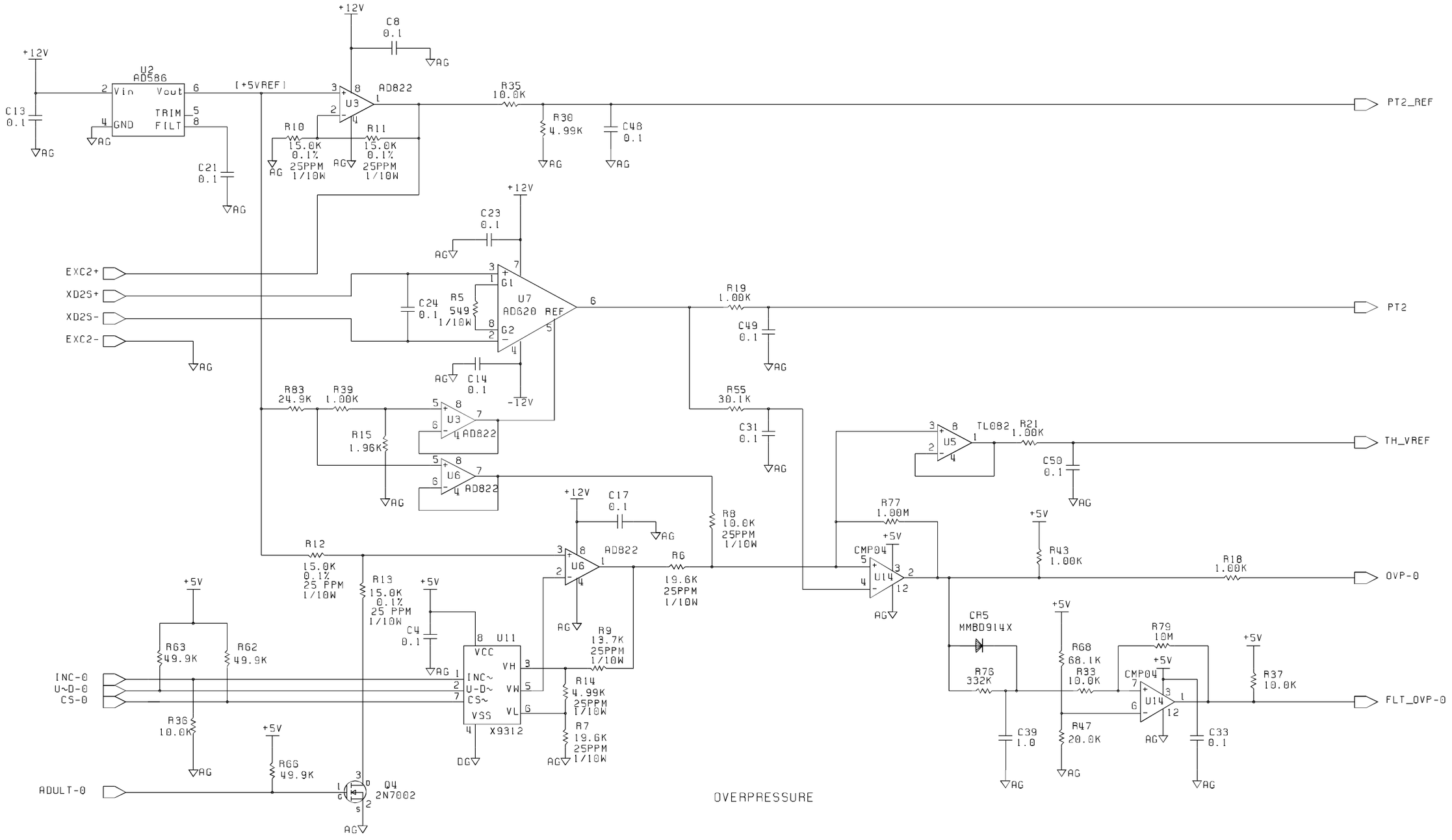
SC315-452 A
NIBP Analog PWA Schematic (1 of 5)



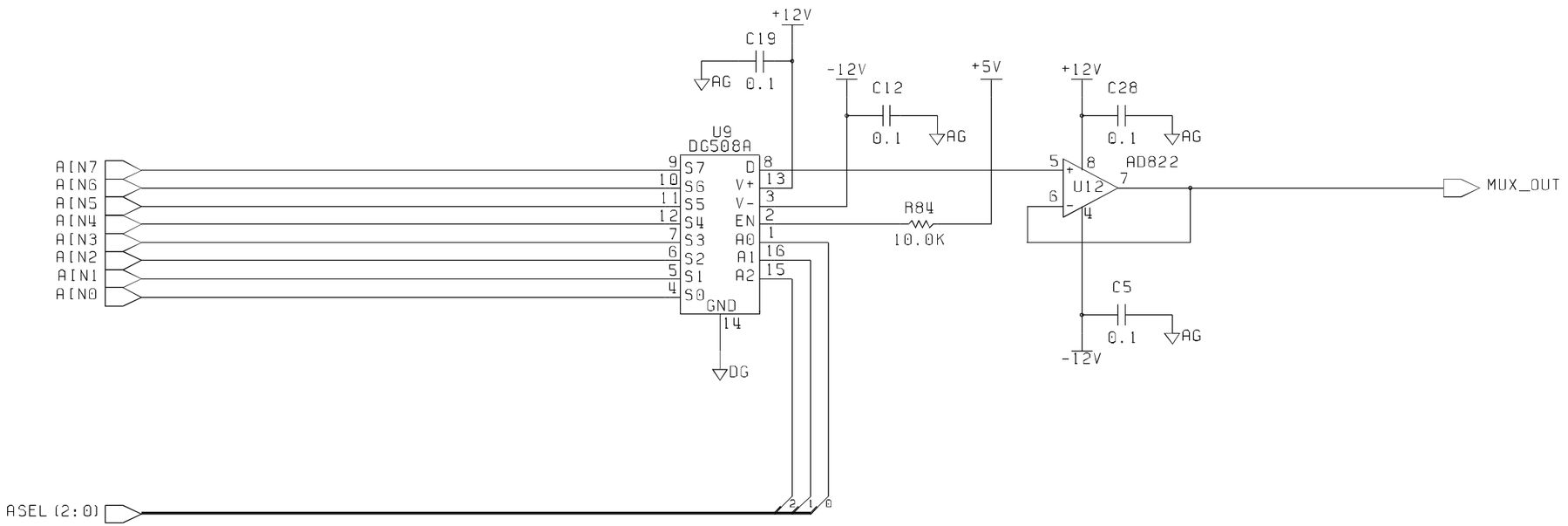
SC315-452 A
NIBP Analog PWA Schematic (2 of 5)



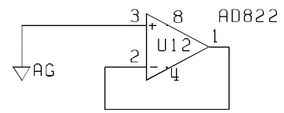
SC315-452 A
NIBP Analog PWA Schematic (3 of 5)



SC315-452 A
NIBP Analog PWA Schematic (4 of 5)



ANALOG_MUX



SC315-452 A
NIBP Analog PWA Schematic (5 of 5)